Clock Synchronization

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Outline

- Time in CPS
- Clock and synchronization fundamentals
- Synchronization protocols
- State of the Art and Issues
- Summary

Synchronized clocks are critical components of many current CPS

Bosch-Rexroth

Veselin Skendzic

Huawei

General Electric

Teletronics

Alan D. Monyelle, USN

Brüel & Kjaer

Synchronized clocks are used to:

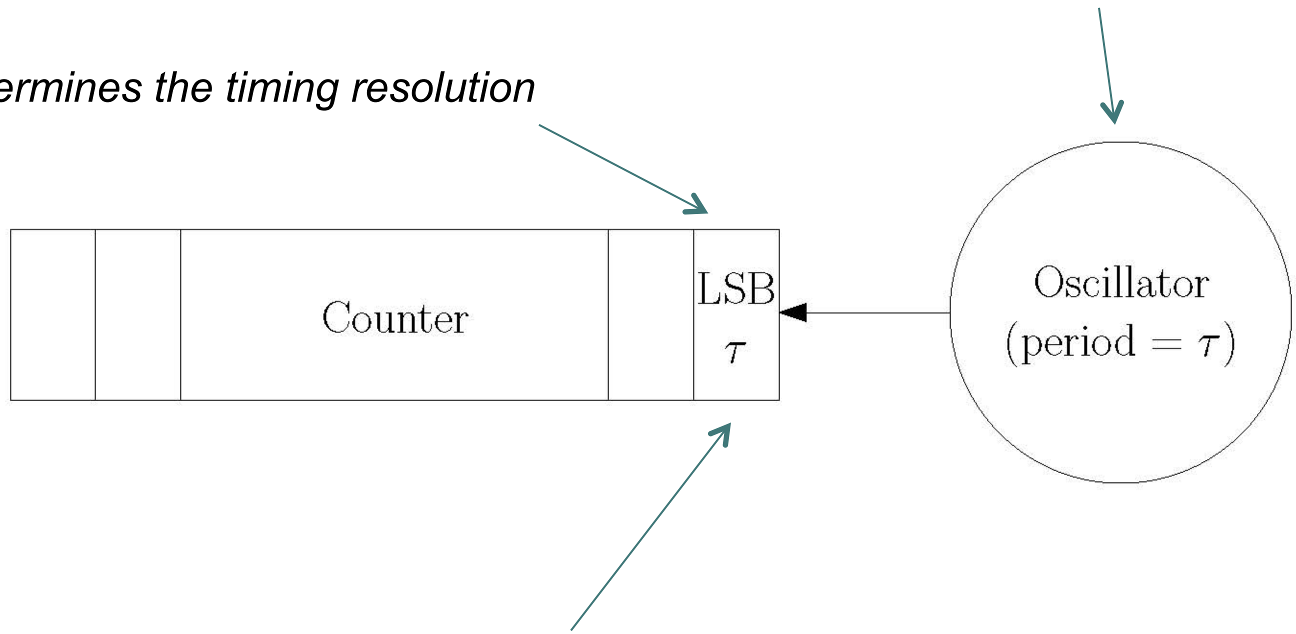
- Implement time-slotted transport protocols
- Timestamp sensor events
- Cause events:
  - Synchronous sensor sampling
  - Synchronous actuation
- Flow control
- Scheduling
- …

Clock basics

Oscillators characterized by:

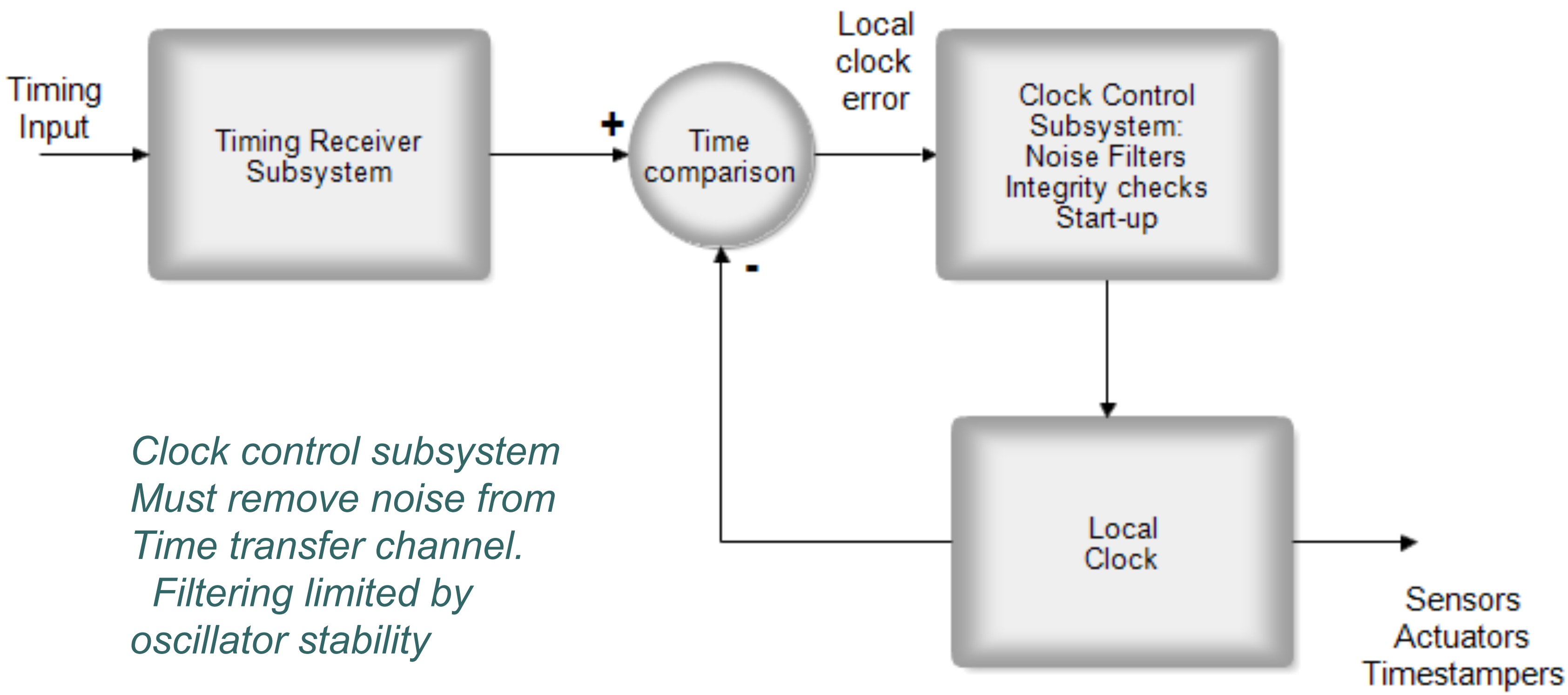
- *Frequency drift => degrades clock accuracy*
- *Noise => degrades clock precision*

LSB determines the timing resolution



Common LSB values are 5-40 ns often corresponding to Ethernet PHY frequencies or FPGA clock rates

Clock basics: steered clock



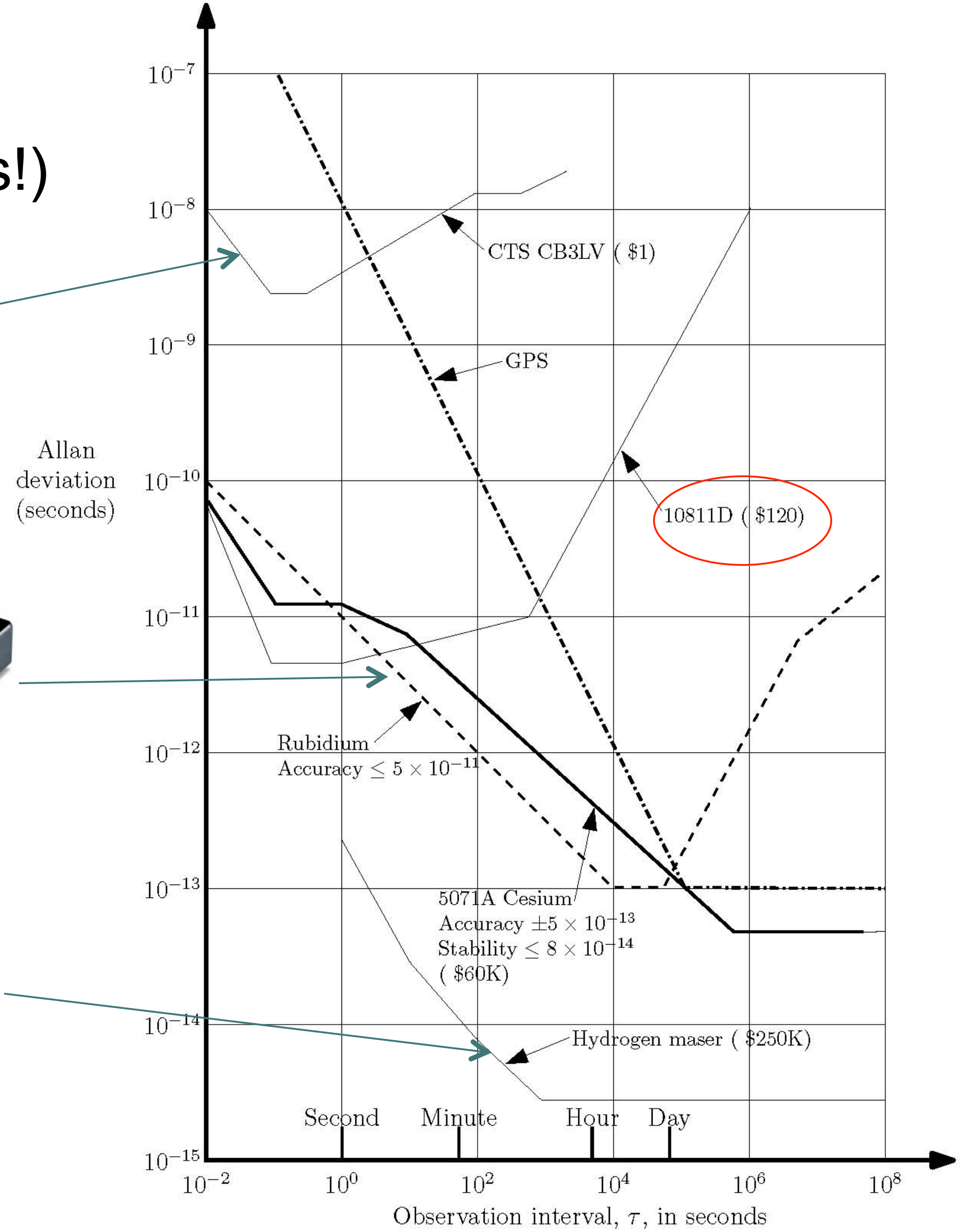
Clock control subsystem Must remove noise from Time transfer channel.
Filtering limited by oscillator stability

Oscillators
(where it all starts!)

CTS Corporation CTS CB3LV ~$1

Symmetricom SA.45s CSAC ~ $1000 120mW, 35 grams

Symmetricom MHM2010 Active Hydrogen Maser Clock ~ $200K, 75W, 475 lbs

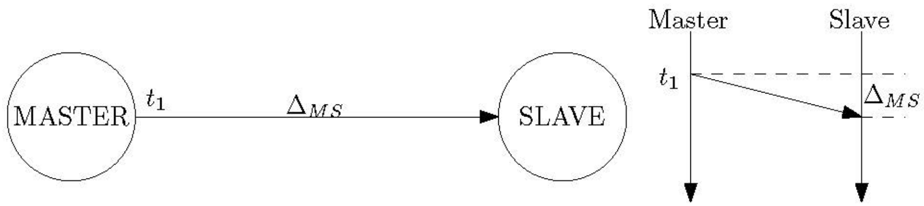


Oscillator attributes

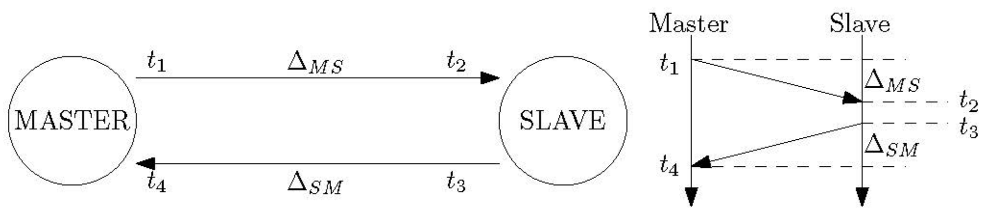
Type	Cost	Integration time	Holdover (5 °C temp change)	Temperature variation
XO	\$1	1 sec	500 ms / day	$1x10^{-4}$ / deg C
TCXO	\$40	100 sec	500 μs / day	$1x10^{-7}$ / deg C
OCXO	\$150	1000 sec	50 μs / day	$1x10^{-8}$ / deg C
CSAC	\$1000	10^4 sec	3 μs / day	$6x10^{-12}$ / deg C
Rb	\$800	10^4 sec	1 μs / day	$1x10^{-12}$ / deg C
Cs	\$50K	>10days	>10 days@10ns	$2x10^{-14}$ / deg C
H-Maser	\$200K	>10 days	>10 days@1ns	$1x10^{-14}$ / deg C

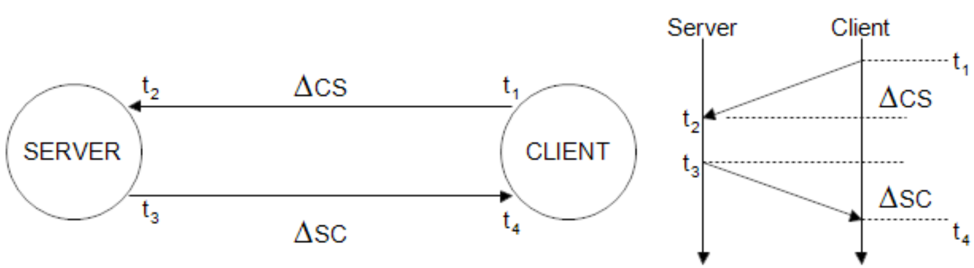
Clock synchronization basics

- One-way protocols (e.g. GPS, IRIG-B)

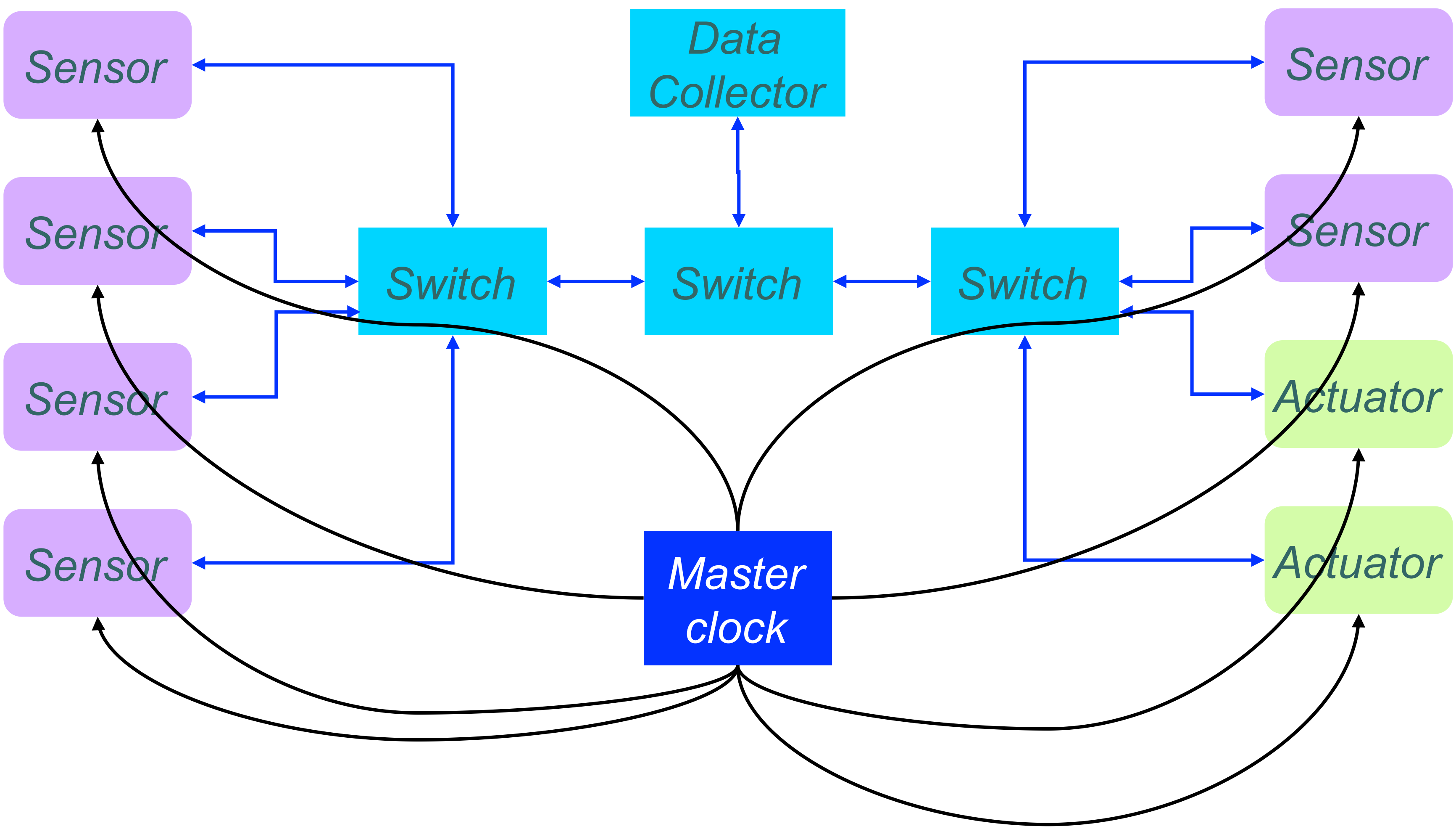


- *Two-way protocols (e.g. PTP, NTP)*

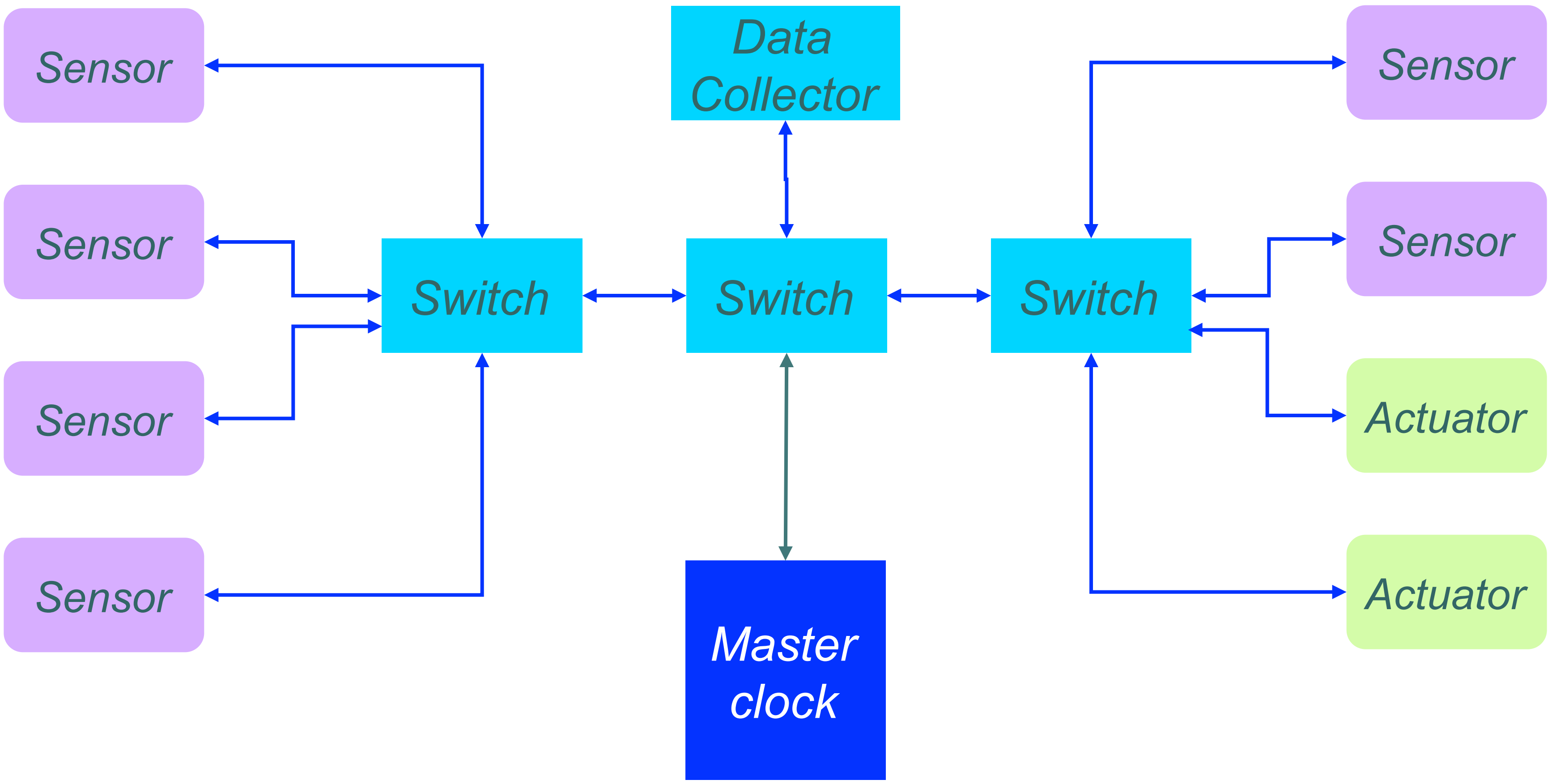




Time Transfer Using Dedicated Timing Infrastructure



Time Transfer Using the Data Network



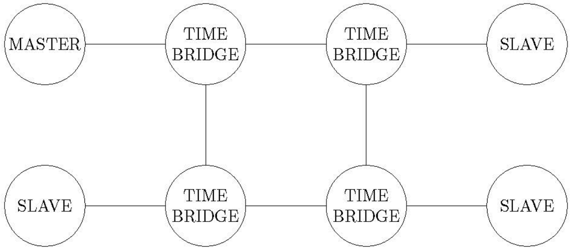
Doug Arnold, John Eidson

Motivation for network based data and time synchronization…

F-18 Aircraft Static Fatigue Test System
Boeing

Image courtesy of National Instruments

Clock synchronization vulnerability

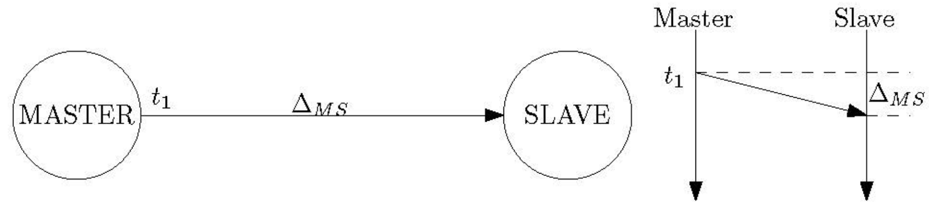


- Protocol absolute accuracy
  - Master (source) accuracy
- Protocol relative accuracy
  - Path length and asymmetry errors
  - Device calibration
- Protocol precision
  - Clock and time bridge jitter
  - Path jitter
- System vulnerabilities
  - Device failure
  - Path failure or reconfiguration
  - Configuration errors

Clock synchronization protocols

- GNSS (GPS, Glonass, Compass, Indian regional, Galileo)
- NTP (and SNTP)
- PTP(and power, AVB, telecom and industrial profiles)
- IRIG-B and related serial time codes
- 1PPS + serial string
- T1/E1 (frequency only)
- DOCSIS Timing Interface
- TTE (SAE AS6802)
- Loran
- WWV

GPS

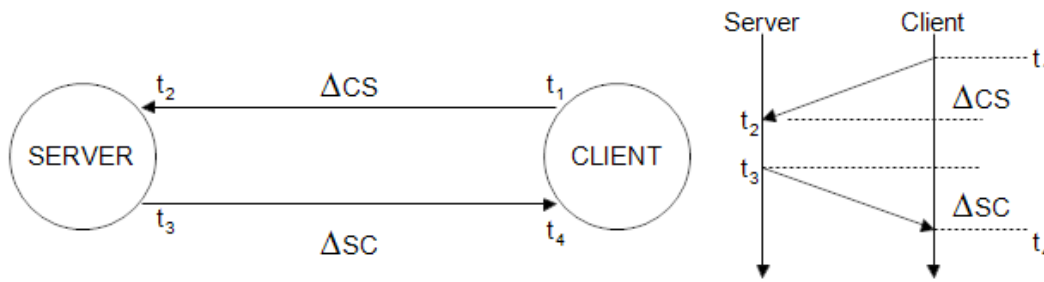


- *Δ_{MS} major corrections are*
  - *Geometric (ephemeris) ~ 65 ms*
  - Ionosphere delay (from model or L1-L2 dispersion) ~ 65 ns
  - *Troposphere delay ~ 5 ns*
  - *Calibration and multipath ~ 10 ns (outdoors)*
  - *Receiver delay calibrations ?*
  - *Master clock relativity corrections ~ 38 μs/day*
- *Accuracy of a GPS-based system*
  - *Easy: 1 μs*
  - *Possible: 50 ns*
  - *Hard: 10 ns or better*

  (data from Judah Levine-NIST):

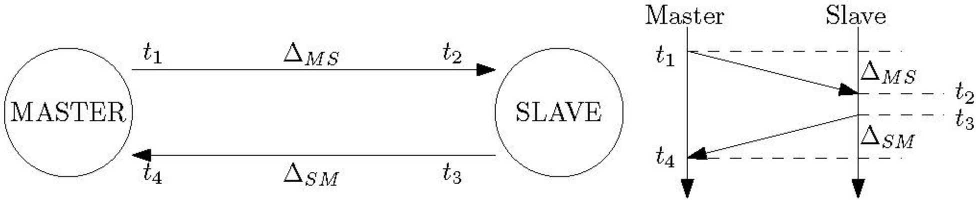
- *Issue: availability indoors/urban canyons*

NTP



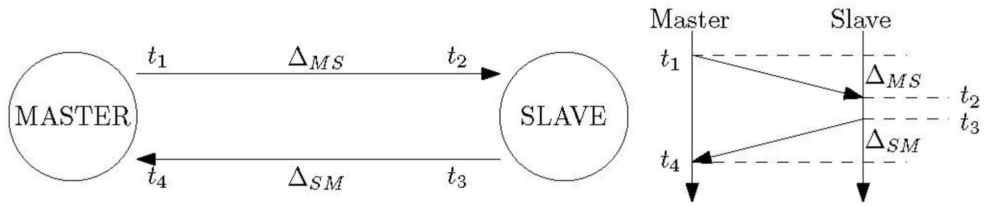
- *Major impairment is path length and asymmetry*
- *Accuracy of a NTP-based system*
  - *Over the Internet typically a few ms*
  - *Over an isolated LAN low μs possible*

PTP



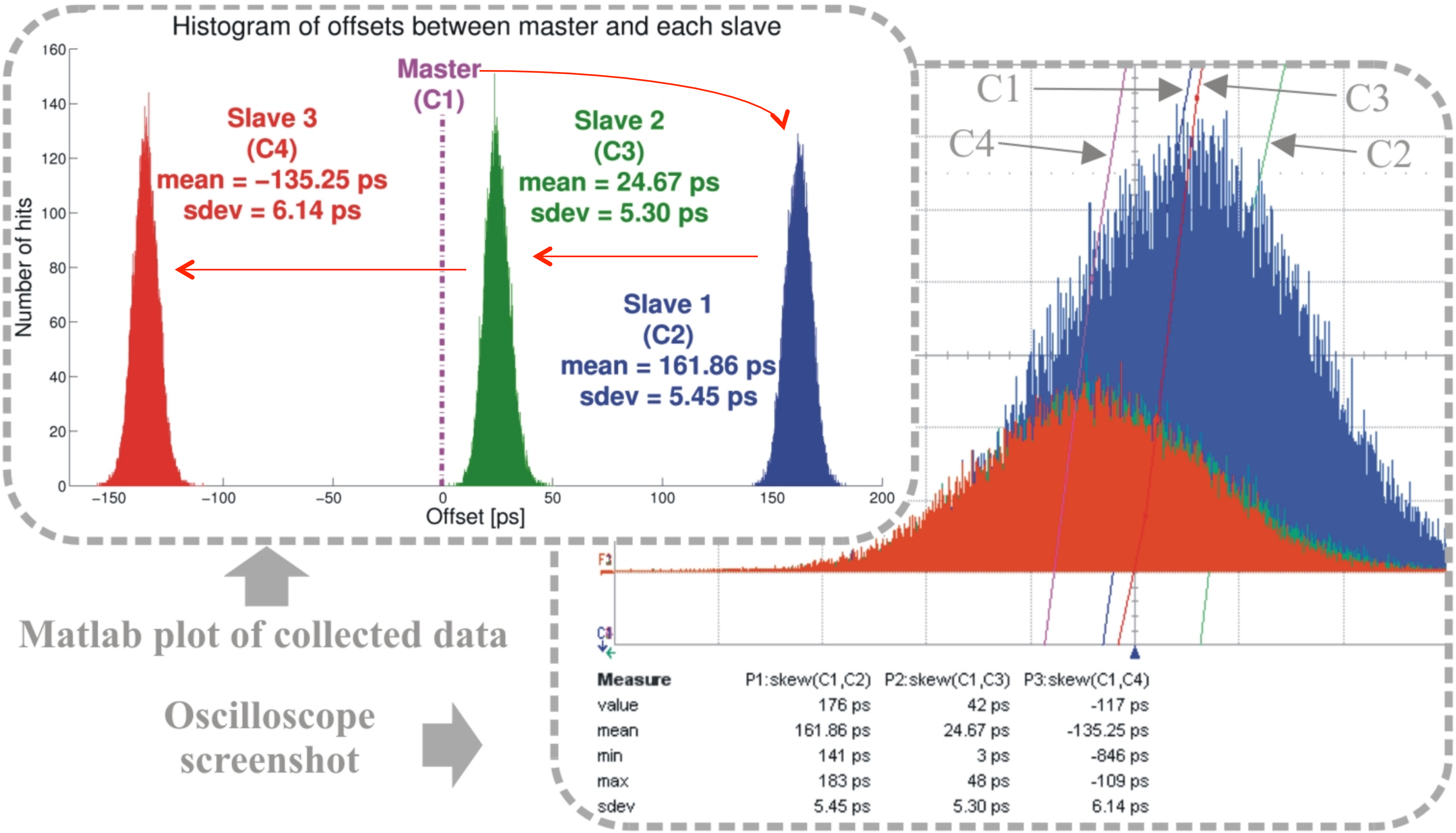
- *Defined by IEEE-1588 standard*
- *Major impairment is path length and asymmetry*
- *Accuracy of a PTP-based system*
  - *Over an isolated LAN without hardware support or time bridges: sub ms to low µs possible but typically traffic dependent*
  - *With hardware support and time bridges (IEEE 1588 boundary or transparent clocks) traffic independent*
    - *Easy: 50-100 ns*
    - *Hard: low to sub-ns level*

PTP+SyncE (ITU-T Std. G. 8262, 2007)



- *Major impairment is path length and asymmetry*
- *Precision is improved by SyneE typically to 10-100 ps range*

White Rabbit Performance: Sub-nanosecond synchronization error over three 5km fiber optic Ethernet links!



Maciej Lipinski, et.al., ISPCS 2011, Munich

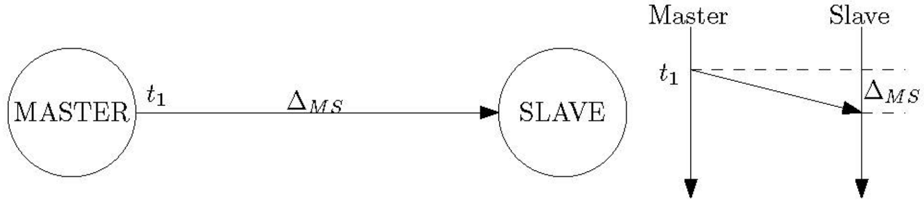
Opportunities, challenges, and issues related to presence of very precise and accurate global time

- *Opportunities: rethink old algorithms and techniques, new applications…*
- *Challenges: handling latency, hardware/software tradeoffs and interfaces, development environments, multiple time sources, heterogeneous networks and protocols*
- *Issues: SyncE not well integrated with other protocols, cost of good clocks and time bridges, security (when applicable), timing hardware/ software interfaces*

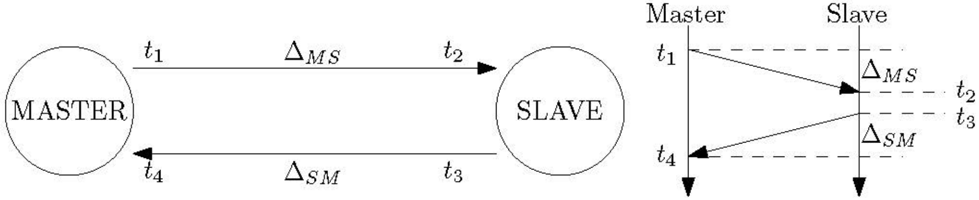
Summary questions

- *What would we do differently if CSACs were 1 ns, 20mw, $15?*
- *What would we do differently if absolute time accurate to <100 ns was available at every Internet port? <5 ns?*
- *Hardware support for clock synchronization is becoming ubiquitous in PHYs and communication systems- what additional hardware support is needed for time-centric applications?*
- *How can precise global time be used to make systems more robust?*
- *How can we make timing itself more robust?*

Discussion



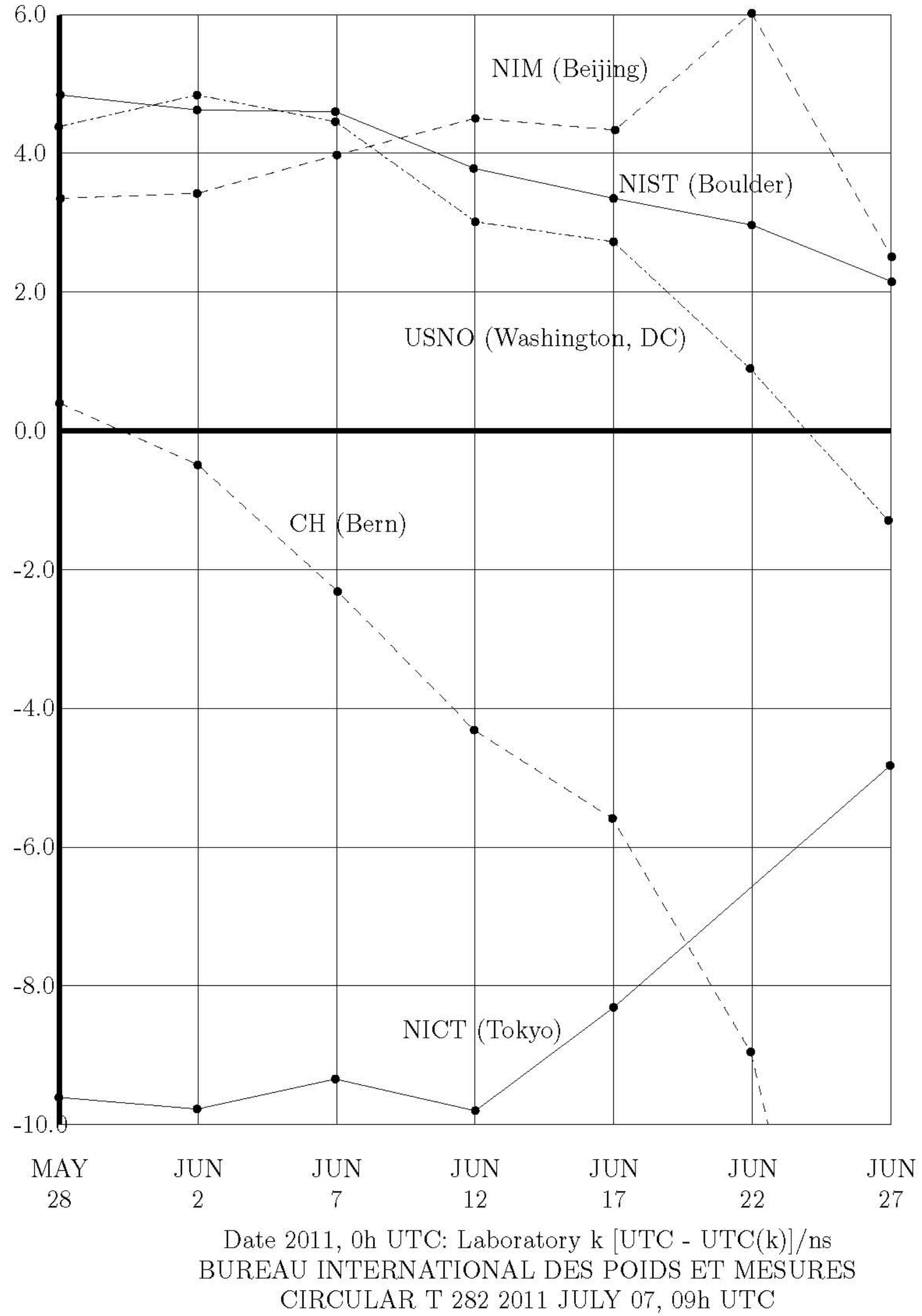
- *One-way protocols depend on knowing Δ_{MS}*
  - *Frequency transfer degraded by Δ_{MS} jitter*
  - *Time transfer degraded by Δ_{MS} jitter and drift*
  - *Δ_{MS} must either be modeled or determined by calibration measurements other than the one-way message*



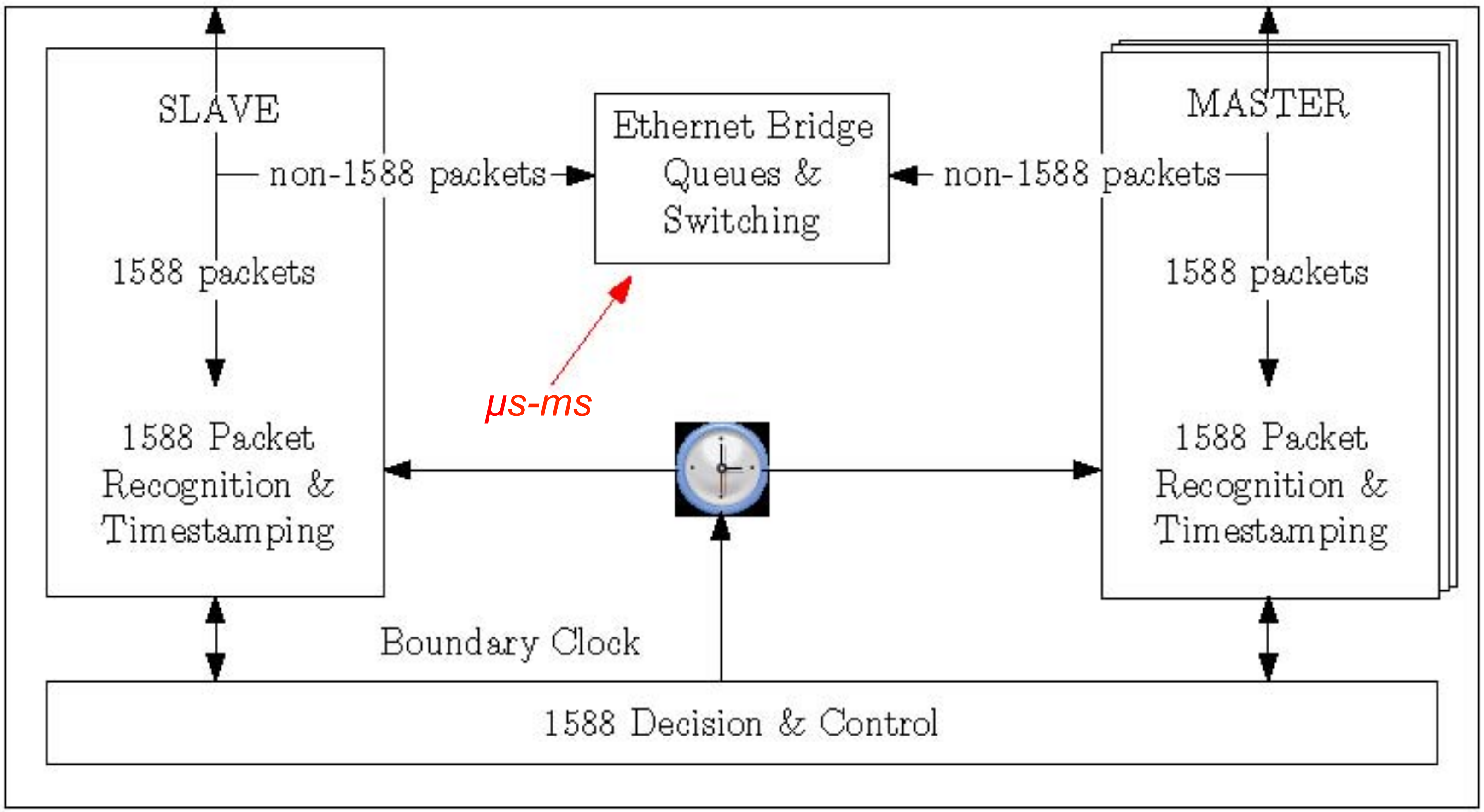
- *Two-way protocols depend on knowing both Δ_{MS} and Δ_{SM}*
- *Time transfer precision degraded by path jitter*
- *Time transfer accuracy by path drift and asymmetry*
- *Path asymmetry must either be modeled or determined by calibration measurements other than the two-way messages*
- *Bridges and routing are major sources of asymmetry*

UTC_i vs. UTC

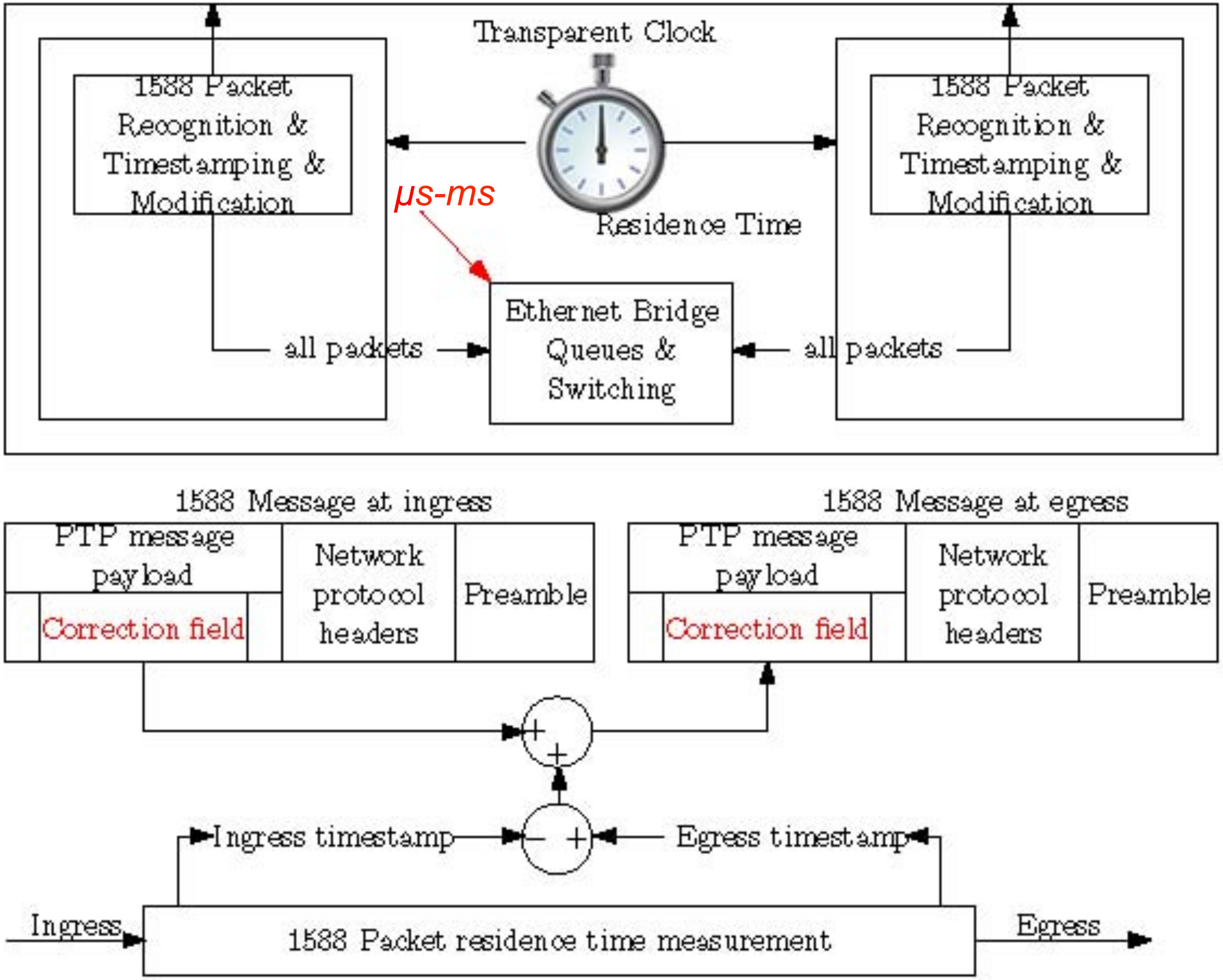
Even atomic clocks drift! Keeping precise and accurate time is very difficult.



IEEE1588 Boundary Clock



IEEE 1588 Transparent Clock

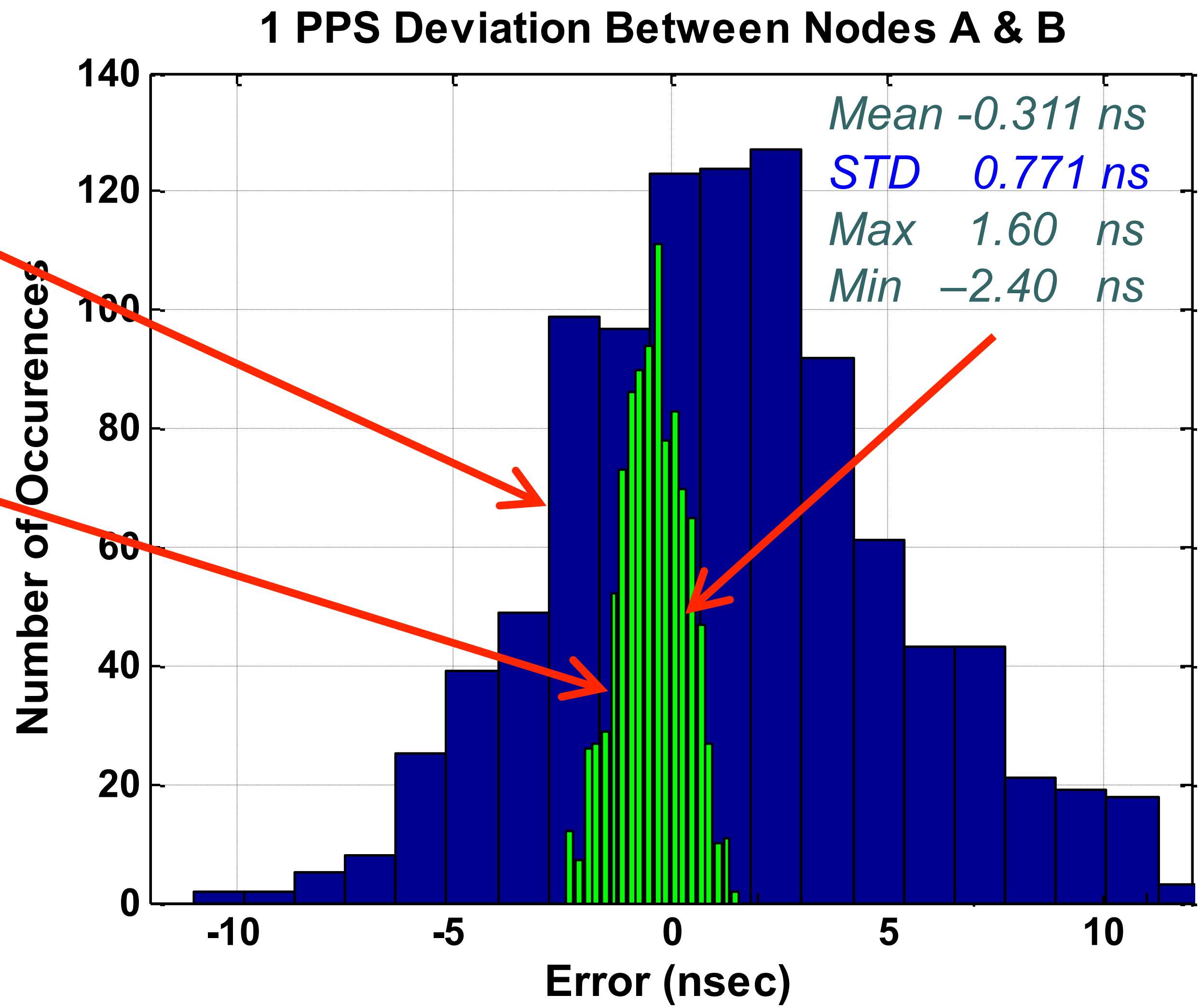


How well can you synchronize?

Typical 8 ns LSB performance

1 GHz design (1 ns LSB)

1000 points over 15 minutes: direct link



From: Update on High Precision Time Synchronization, Vook, et.al., IEEE-1588 Conference, Zurich, October 2005

IEEE 1588v2/PTP and SyncE/ITU-T G.8261

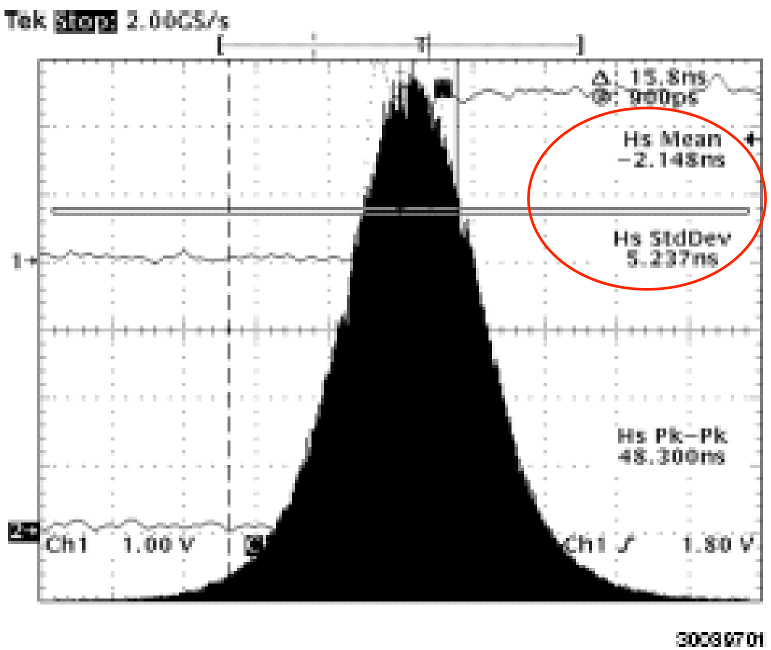


FIGURE 7. Master to Slave 10 MHz CLK_OUT Synchronization with Synchronous Ethernet Mode Disabled

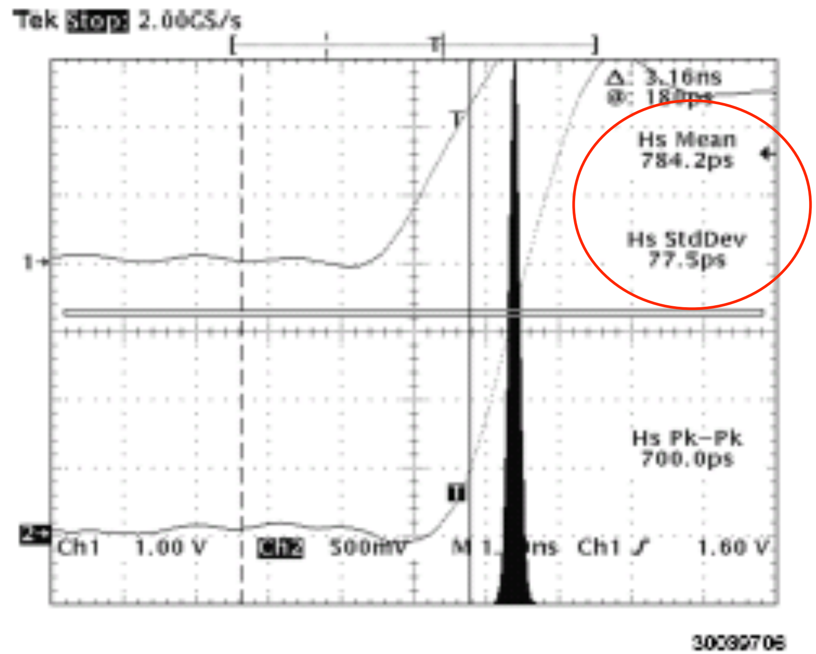
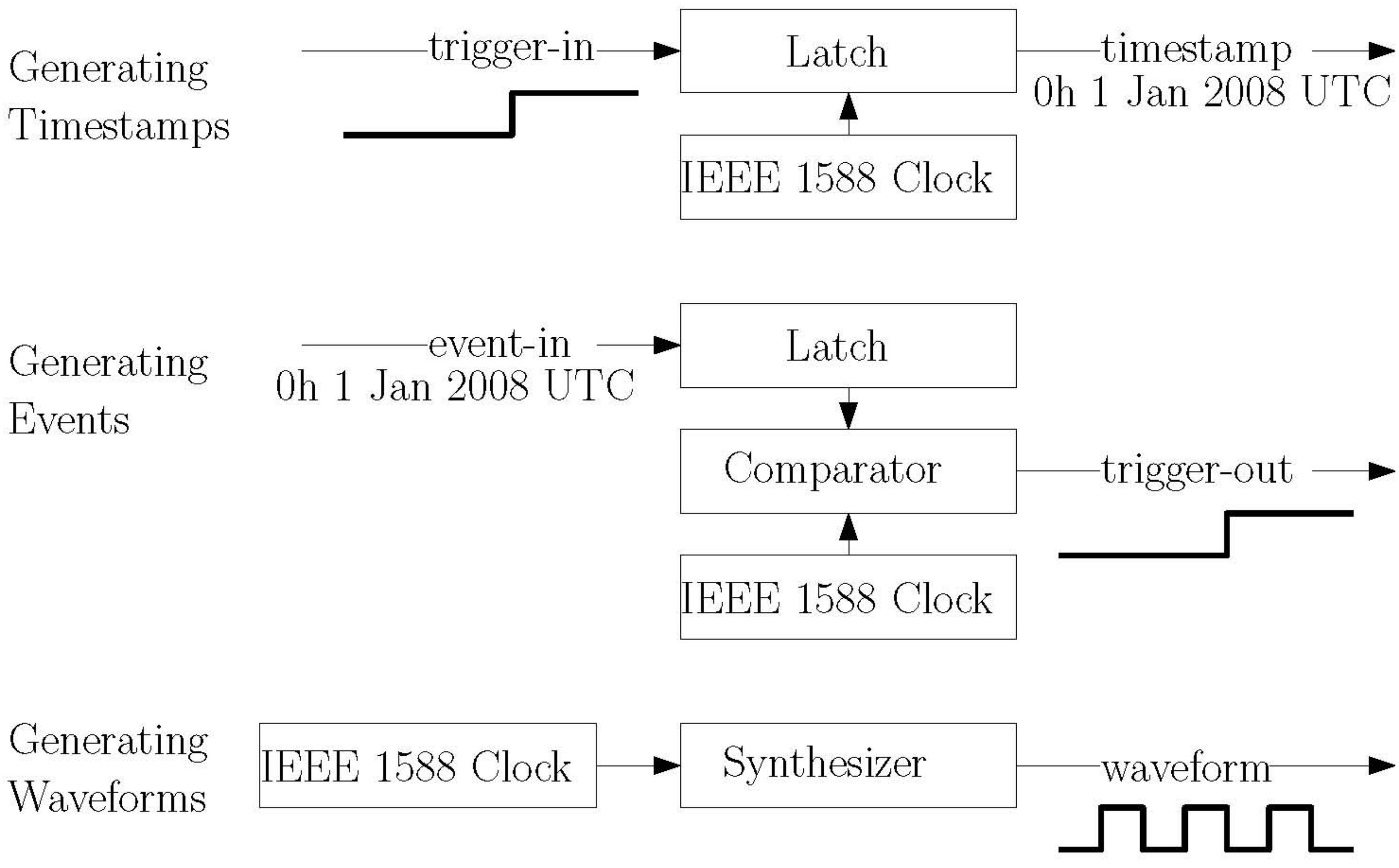


FIGURE 10. Master to Slave 10 MHz CLK_OUT Synchronization with Synchronous Mode Enabled and Crystal Slave Reference Clock

From: "DP83640 Synchronous Ethernet Mode: Achieving Sub-nanosecond Accuracy in PTP Applications, National Semiconductor Application Note 1730, David Miller, September 2007

How do you use a synchronized clock?
(all 3 forms supported in DP83640 PHY chip)



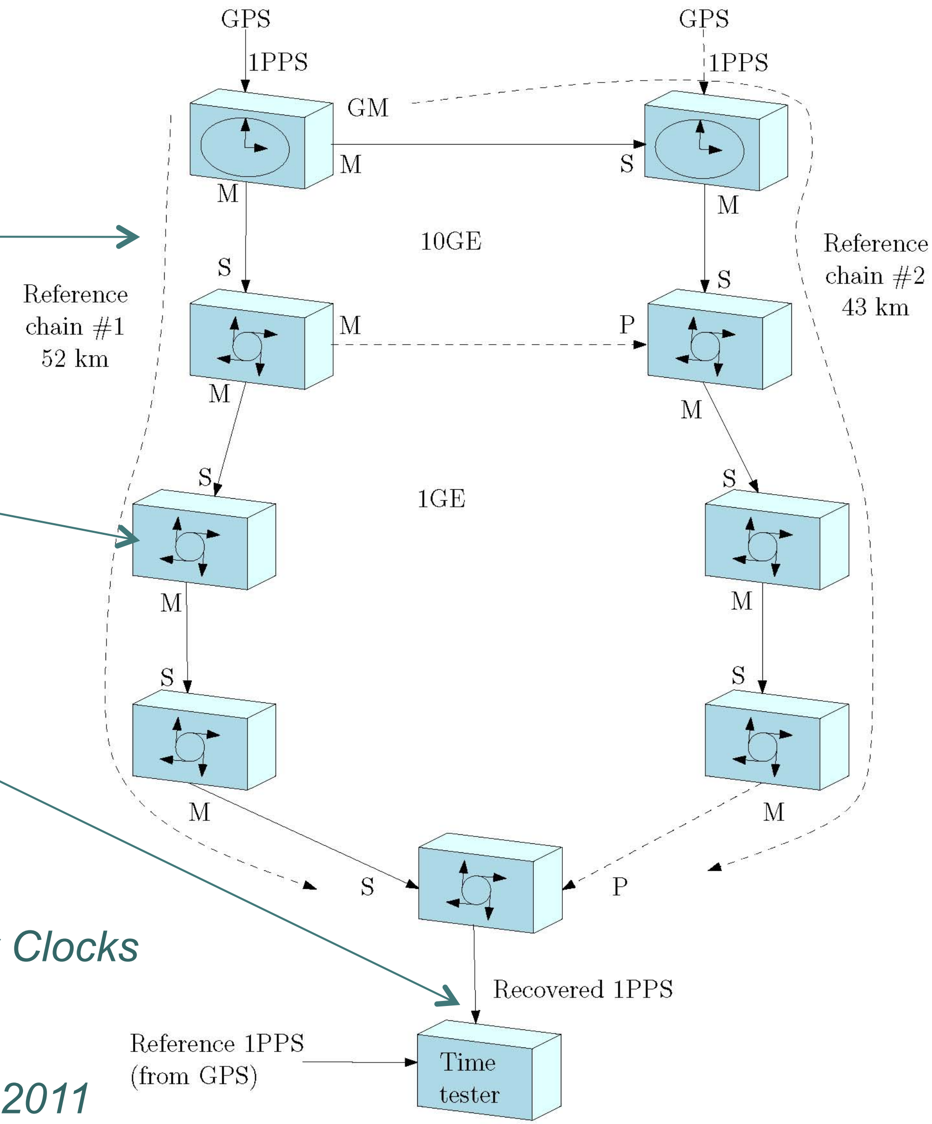
Synchronization requirements for wireless air interface technologies

Technology	Frequency Accuracy	Phase Accuracy
GSM (2G)	±50 ppb	Not required
UMTS	±50 ppb	Not required
CDMA 2000	±50 ppb	±3.0 µs
WCDMA	±50 ppb	±1.25 µs reference to BTS ±2.55 µs between base stations
Pico RBS (WCDMA and GSM)	±100 ppb	±3.0 µs

Based on a Juniper Networks white paper- 'Synchronization Deployment Considerations for IP RAN Backhaul Operators'

Telecom time transfer field trial in China

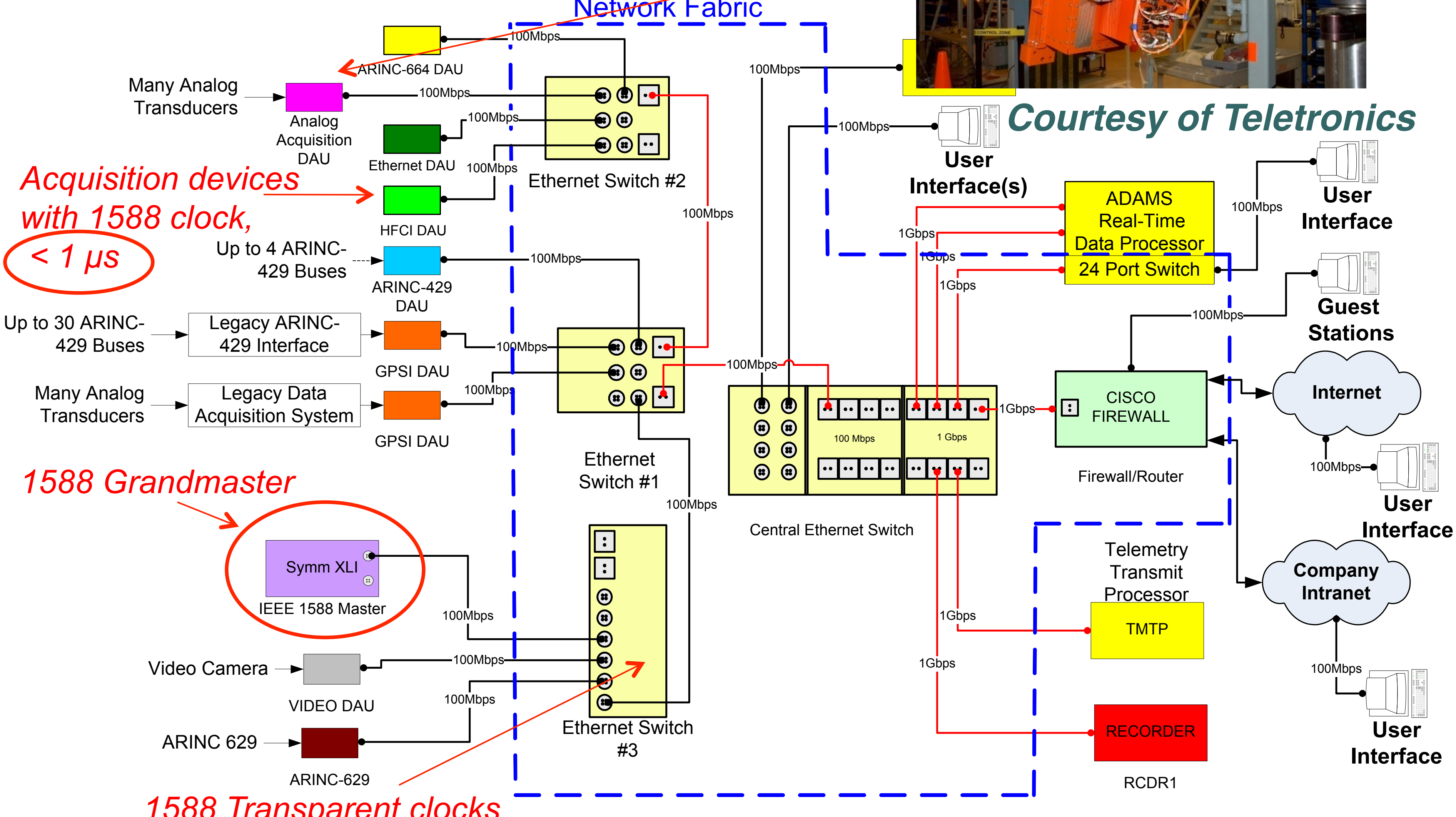
- Each chain had 15 boundary clocks
- BCs used SyncE for frequency and 1588 for time transfer
- Accumulated error < 3 μs requirement for TD-SCDMA



From "Using IEEE 1588 and Boundary Clocks for Clock Synchronization in Telecom Networks"- Ouellette, et.al. IEEE Communications Magazine • February 2011

Aircraft telemetry

(courtesy Lee Eccles, Hung Mach, Larry Malchodi of Boeing)



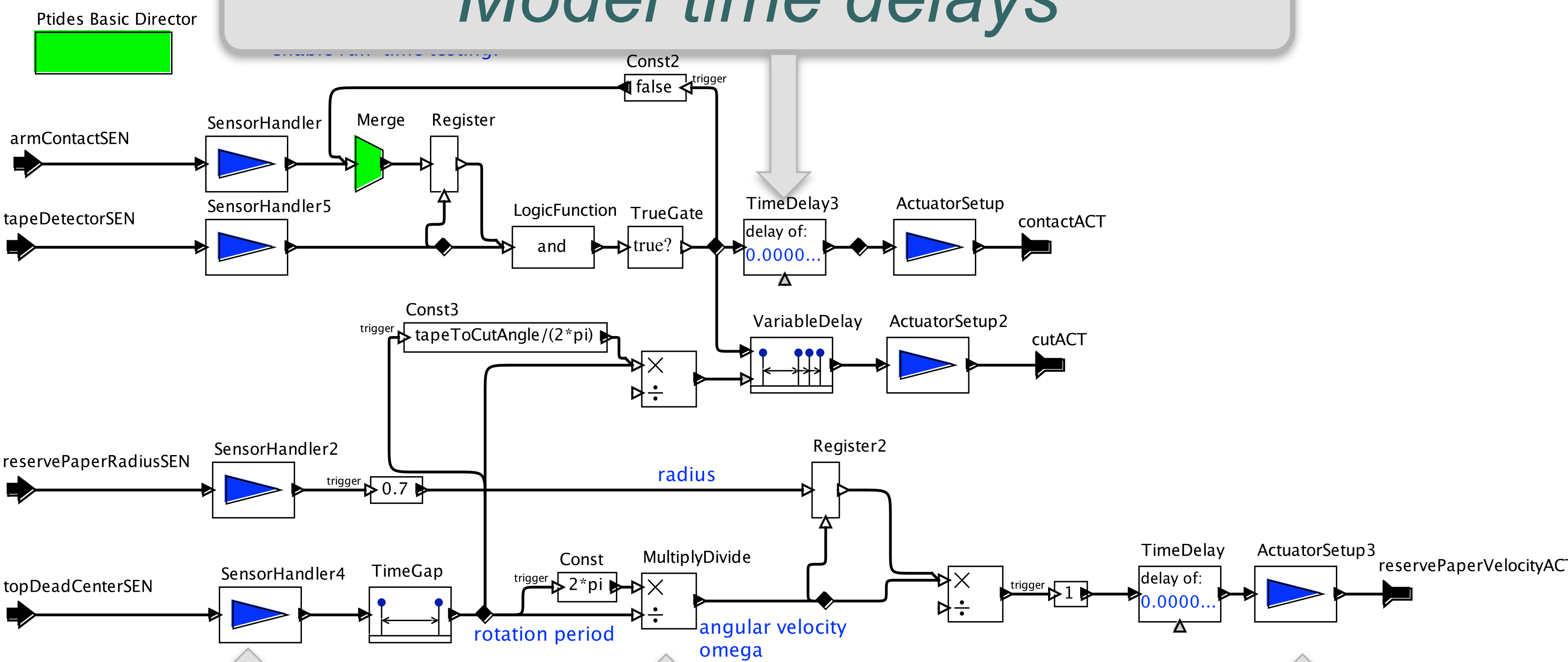
CERN's White Rabbit Project

(*based on "White Rabbit: a PTP Application for Robust Sub-nanosecond Synchronization"- Maciej Lipinski, et.al., ISPCS 2011 Munich*)

- Goal: Develop an alternate timing and control system for the General Machine Timing at CERN
- Synchronization of up to 2000 nodes with sub-nanosecond accuracy, an upper bound on frame delivery and a very low data loss rate
- Based on and compatible with Ethernet (IEEE 802.3), Synchronous Ethernet (ITU-T Std. G.8262, 2007) and IEEE 1588-2008.
- For sub-nanosecond EVERYTHING matters: oscillators; media, PHY, board asymmetry, temperature, …

T-REX Controller

Model time delays



Sensors *Computations* *Actuators*

Renesas vs. XMOS: Measured I/O timing