Multi Time-scale Real-time Simulations and Hardware-in-the-loop Methods for the Research of Energy and Power Structures for Mission Critical Systems

For mission critical systems, such as mircogrids for military camps and power systems onboard ships, aircrafts, and spacecrafts, high fidelity multi time-scale real-time (RT) simulation is needed to study system behavior, subsystems interactions, and component performance.

In the RT simulation of a complex energy system, the necessity of modeling large time scale (ms-s) systems arises from the characteristics of renewable energy resources and energy and power management on different types of land, sea, and air vehicles. On the other hand, electric machines and associated high bandwidth control algorithm demand modeling at a medium time scale (us-ms). Finally, the power electronics devices that connects energy resources with the electrical machines work at an even smaller time scale from picoseconds to nanoseconds. Even though commercial RT hardware units are capable of modeling large complex systems, the total amount of CPU power, needed memory, etc. make it not a cost-effective solution [1]. The introduction of renewable energy such as solar and wind calls for new methods and models to be designed which reduce system complexity [2-6].

Furthermore, with the introduction of high speed wide bandgap power switching devices, the switching frequency of power converters can be increased significantly. To study the transient behavior of these converters, the time step of the RT model should be much smaller than the converter's switching time step, i.e. $T_s << T_{sw}$. Typical CPU based RT simulation can only achieve a minimum time step of $T_s \geq 10$ μs, caused by the large bus latencies. One way to decrease this time step as is to utilize GPUs. However, they inherit the same drawbacks that CPU based solutions have. At this time, the minimal time step of GPU based simulation is around 1 us [7]. Thus, for picosecond and nanosecond based simulation for WBG devices, new platforms and modeling methods are still yet to be found.

More challenges are presented during the interconnection of the RT model to the physical equipment under test (EUT). With EUT, RT simulation based Control Hardware in the Loop (CHIL), Power Hardware in the Loop (PHIL), and System in the Loop (SITL) need to be implemented. And, this implementation should be "ideal." However, the input / output signals from the RT model range from -20 to 20 V and are incapable of delivering or receiving high power from the EUT. A power amplifier is therefore needed as the link between these two systems. The dynamics added by these amplifiers can deteriorate the fidelity and even caused instability in an otherwise stable system. This interconnection is shown in Fig. 1 where for an ideal system $G_{PA}(s) = 1$. Power amplifiers are limited by their bandwidth and voltage / power capabilities. Another type of interconnection is System in the Loop or SITL. This type of connection is usually defined for network simulators and is used in parallel to another RT system, or the actual communication devices. Typical SITL systems such as the ones available through OPNET [8], offer great network modeling and flexibility, but the Ethernet interconnection needed, with a typical latency of ~ 2ms, deteriorates the performance and fidelity needed. In CHIL, the model fidelity is the most important factor affecting the accuracy of this test as well as for FPGA base simulation the bandwidth of the DAC affects the signals seen by the controller.

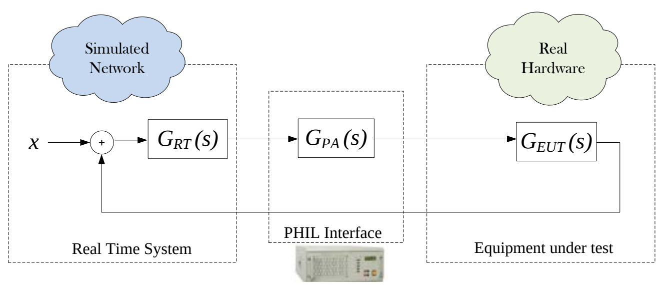

Figure 1 PHIL Setup including power amplifier

Table 1 Challenges in interconnection between the RT model and EUT

Physical Interconnection	Issues
PHIL	Power amplifier latency - bandwidth
	Stability and accuracy
SITL	Latency in Ethernet links
CHIL	Fidelity of the RT model
	DAC, ADC bandwidth

As stated above, there are remaining challenges in real-time simulations of energy systems at all time scales. When high fidelity simulation is needed to study interactions between sub energy systems of different time scales, proper method is yet to be established. Also, the three main hardware-in-the-loop methods all have inherent problems to be solved to improve execution accuracy, stability, and fidelity. Thus, the research on RT simulation and HIL is still at its dawn. The challenges ahead call for extensive interdisciplinary research efforts from the CPU community.

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