

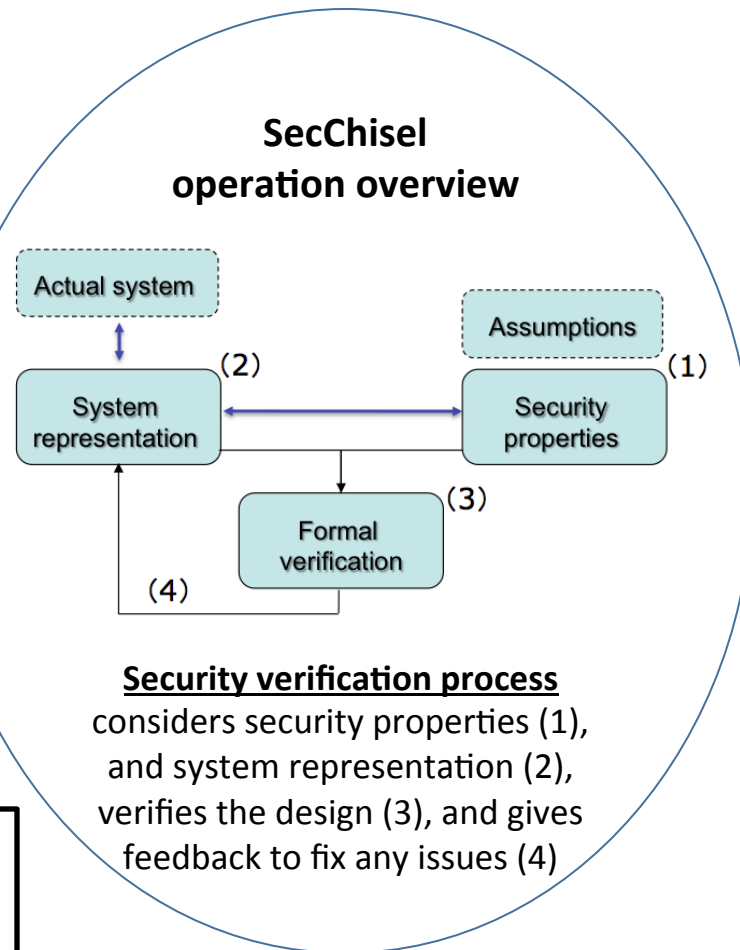
Practical and Scalable Security Verification of Security-Aware Hardware Architectures

Challenge:

- How to perform security verification of a processor or a whole computer architecture at the design time?
- How to semi-automatically combine design specification and security verification?

Solution:

- Designing a new language, SecChisel, for hardware construction and information flow analysis.



Scientific Impact:

- Leveraging tools familiar to computer architects, i.e., Chisel hardware construction language, for ease of adoption.
- Adding new security tags and lattice-based hierarchy of the tags to enable security analysis of information flow in the design.

Broader Impact:

- Computers form the backbone of any modern society, and often process large amounts of sensitive and private information, ensuring computer hardware is secure at design time is critical to security today's computing infrastructure.
- The research involves international collaborators to enhance impact of the work.

Prof. Jakub Szefer, W. Xiong, and S. Deng
Yale University (NSF Grant #1524680)

Prof. Onur Demir and D. Gümüšoğlu
Yeditepe University, Turkey

Prof. Ruby B. Lee and T. Zhang
Princeton University (NSF Grant #1526493)