PostDoc position on "Real-Time Memory Management in Latest-generation CPU+FPGA SoCs" (TUM Munich, Germany)

Submitted by Anonymous on Tue, 06/04/2019 - 9:18am

Brief Info:

- Institute: Chair of Cyber Physical Systems in Production Engineering, Technical University of Munich.
- (See http://www.professoren.tum.de/en/caccamo-marco/)
- We are currently looking for motivated a Post-doctoral researcher who would like to work at TUM, Munich in collaboration with Boston University (BU), USA
- Contacts: email mcaccamo@tum.de and rmancuso@bu.edu

Scientific Context:

Modern multi-core System-on-Chip (SoC) technologies in embedded computing systems pose new challenges for safety critical and real-time applications due to (i) increased temporal coupling between processing cores, (ii) higher degree of software integration and (iii) increased uncertainty in the hardware timing model that is used in the development and certification of embedded software for safety critical real-time systems (like avionics, autonomous automotive systems, production robots, etc.). In multi-core architectures, coupling across distinct software partitions arises because of shared hardware resources (like cache, main memory, I/O, and dedicated hardware engines), and result in loss of composability. In other words, when two software components are composed (i.e., simultaneously executed), the effect that one has on the performance of another can be significant, resulting in unexpected temporal behavior. The problem of inter-core performance interference in multi-core architectures is well known and has been largely studied in literature [1, 2].

Software-level performance isolation techniques have been extensively investigated, but they come with high overheads, work at a coarse granularity, and often require complex analysis techniques to derive real-time guarantees [3]. Recently, however, hardware manufacturers have started to integrate programmable logic (FPGA) onto multi-core SoCs. The tight coupling of FPGA and traditional CPUs opens the road to a whole new set of techniques to perform smart memory resource management. In fact, one can define new hardware modules in charge of implementing high-level policies on memory traffic that are enforced at the granularity of individual memory transactions.

Research:

The PostDoc will work on resource management for real-time heterogeneous SoC. He/She will research, develop, and evaluate innovative resource management solutions to address or mitigate contention at several levels (interconnects, caches, memories, etc). The candidate will closely work with other PostDocs and help supervise Master and PhD students. While based mostly in TUM, the candidate will also coordinate and interact either in person or remotely with the research team at BU.

Requirements:

The candidate is required to have a PhD degree in computer science or electrical computer engineering and preferably should have a strong background in computer architecture and FPGA programming, as well as in real-time systems theory and operating systems. Efficient communication skills (oral and written) in English are required.

Work position and application:

The position is full-time and paid according to pay scale "TV-L, E13 or E14", depending on the qualifications. The position is open to applicants worldwide.

Your complete application consists of the following documents, which should be sent as PDF files:

- CV with photo
- One-page cover letter (clearly indicating available start date as well as relevant qualifications, experience and motivation)
- University certificates and transcripts BSc, MSc, and PhD degrees)
- Contact details of up to three referees
- List of publications and possibly an English language certificate

All documents should be preferably in English.

References:

1. H. Kim, D. de Niz, B. Andersson, M. Klein, O. Mutlu, and R. Rajkumar. Bounding memory interference delay in cots-based multi-core systems. In 2014 IEEE 19th Real-Time and Embedded Technology and Applications Symposium

(RTAS), pages 145-154, April 2014.
2. L. Sha, M. Caccamo, R. Mancuso, J.-E. Kim, M.-K. Yoon, R. Pellizzoni, H. Yun, R. Kegley, D. Perlman, G. Arundale and R. Bradford, "Real-Time Computing on Multicore Processors", IEEE Computer, Vol. 49, Issue 9, pp. 69-77, September 2016.
3. A. Agrawal, R. Mancuso, R. Pellizzoni and G. Fohler, "Analysis of Dynamic Memory Bandwidth Regulation in Multi-core Real-Time Systems," 2018 IEEE Real-Time Systems Symposium (RTSS), Nashville, TN, 2018, pp. 230-241.

? Post-doctoral Fellow in Embedded Information Processing Fully-funded PhD position at Inria Lille (France) ?

Position Announcements
