CPS: Synergy: Thermal-Aware Management of Cyber-Physical Systems

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Motivation

- Cyber-physical processors work in harsh environments and often suffer very high operating temperatures.
- High temperatures accelerate processor aging and increase failure rate.
- Effective thermal-aware management is required to meet the computational demands of the application while reducing processor thermal stress.

Failure Sources

- Electro-migration
- Dielectric breakdown
- Negative bias temperature instability

All strongly dependent on temperature

Our Approach

Controlled Plant:
- Current state
- Dynamics
- Desired trajectory
- Safety envelope

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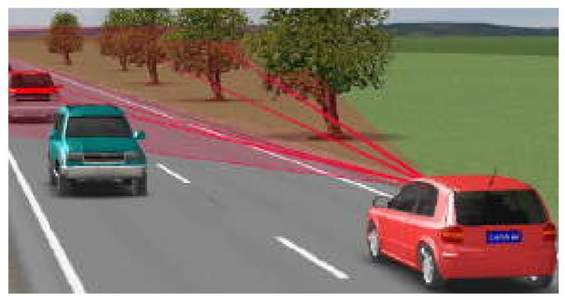
- Dynamic computational workload and core assignment
- Core reconfiguration

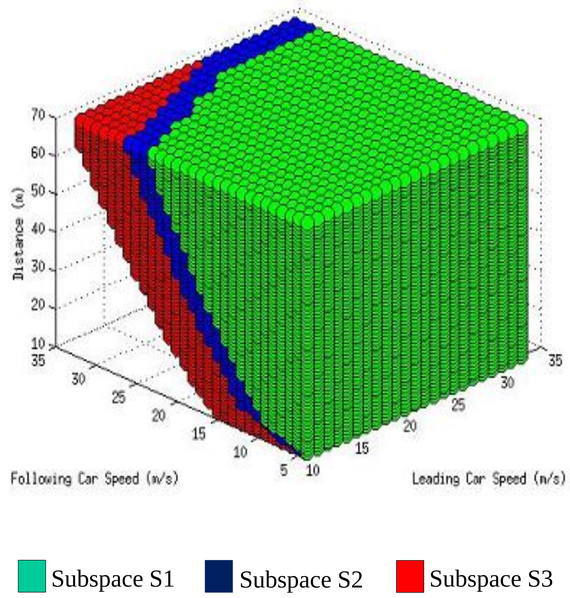
Balance quality of control against thermal stress

Plant Safe State Space

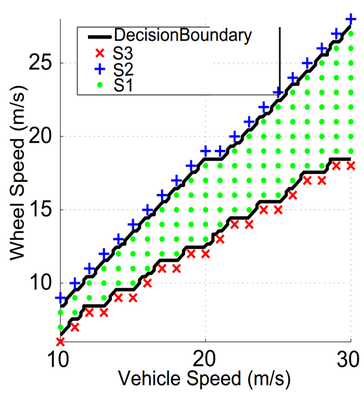
- S1: No fault tolerance needed
- S2: Only Fault detection needed
- S3: Full fault masking required

Case Study: Car Platooning

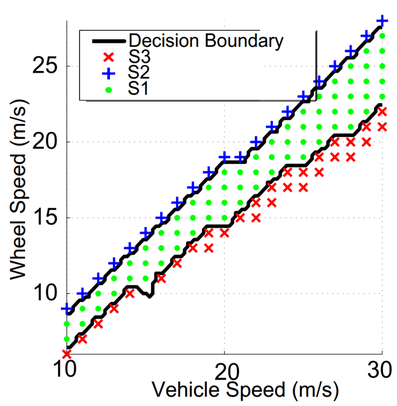




Safe State Spaces: ABS



Road Friction Coefficient 1.0



Road Friction Coefficient 0.8

Thermal-Aware Task Scheduling

Heterogeneous multi-core platform
- Big Core (BC): 4-way Out-of-Order
- Small Core (SC): 1-way In-order

Key Observation: Greater thermal gains from slowing down (DVFS) program execution phases with high IPC ➡ high thermal impact

Steps:
- A1: Assign as much workload to small cores as possible
- A2: Assign tasks with smaller thermal impact to big cores
- A3: Perform task reassignment when tasks finish earlier than WCET
- A4: Apply DVFS preferentially to code segments with higher thermal impact