CPS: Small: RUI: CPS Foundations in Computation and Communication (CPS-0932113)

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CPS applications require a network consisting of multiple computational-sensing nodes scattered throughout an area of interest. We proposed a secure, power-efficient, and latency-limited communication scheme for CPS networks. This communication scheme consists of 1) a multipath multicast algorithm that efficiently relays information to a group of CPS nodes and 2) a data acquisition technique that performs in-network processing to reduce large streams of raw data into useful aggregated information.

Our proposed multicasting algorithm is different from the existing multicasting algorithm, as it is neither tree-based nor mesh-based. This algorithm was designed with simplicity, energy-efficiency, and reliability in mind. Our algorithm combines the best of multicasting, which we have based on multi-path Multicast Operation of the Ad-hoc On-Demand Distance Vector (MAODV), with the best of Distributed Source Coding (DSC), which incorporates and uses ideas from rateless coding. By adding DSC using rateless codes on top of multi-path MAODV, the transmission load is distributed more evenly among the CPS nodes and the communication is more robust against link losses. Unlike existing algorithms, receiving any subset of the encoded packets will help the destination nodes achieve full recovery of the original information.

Our data aggregation algorithm exploits both spatial and temporal correlations between sensor readings to reduce the total number of transmissions. For spatial correlation, we propose a compressive sensing (CS) technique that uses rateless coding and random walk. The rateless coding generates a random measuring matrix that is independent of routing algorithms and is incoherent with any sparsity matrix with high probability. Equipping the CS-based algorithm with random walk enables the collection and combination of a sufficient number of sensor readings without significantly increasing the inter-communication cost. Then, we enhanced our algorithm to reactively change its compression rate using a sliding scale window. For this purpose, our proposed algorithm changes its compression rate to adapt to event-based variations in the sensor readings. In case of events that significantly change the signal readings, the algorithm generates more measurements to guarantee recovery of signal at the base station.

Modern processor architectures sacrifice timing predictability for increased average computational throughput. Branch prediction, multi-level memory hierarchies, out-of-order execution, and data forwarding all make accurate execution time predictions impossible. As accurate timing predictions are required for task scheduling, we have developed a Precision Timed (PRET) processor based on an existing open source RISC processor with a three-stage pipeline. By interleaving instructions from different threads onto a new six-stage pipeline, all data dependencies can be removed, simplifying the architecture and restoring timing predictability while retaining the throughput advantages of a deeper pipeline. These modifications increase the overall throughput by 70% with only a 35% increase in area.

Scheduling is handled by a dedicated hardware module that provides for cycle-by-cycle thread scheduling. Threads are placed into one of three memory-mapped priority queues by the operating system. The hardware, interfacing with these queues, determines which thread will run in the subsequent clock cycle, considering the priority of threads that are ready-to-run. This cycle-by-cycle scheduling will enable deterministic, single-cycle interrupt latency, an attribute of importance in CPS. By migrating traditional OS functions into hardware, OS context switches are minimized, reducing timing variability.