

Enabling Robust, Secure and Efficient Knowledge of Time Across the System Stack (Start Date: June 2014)



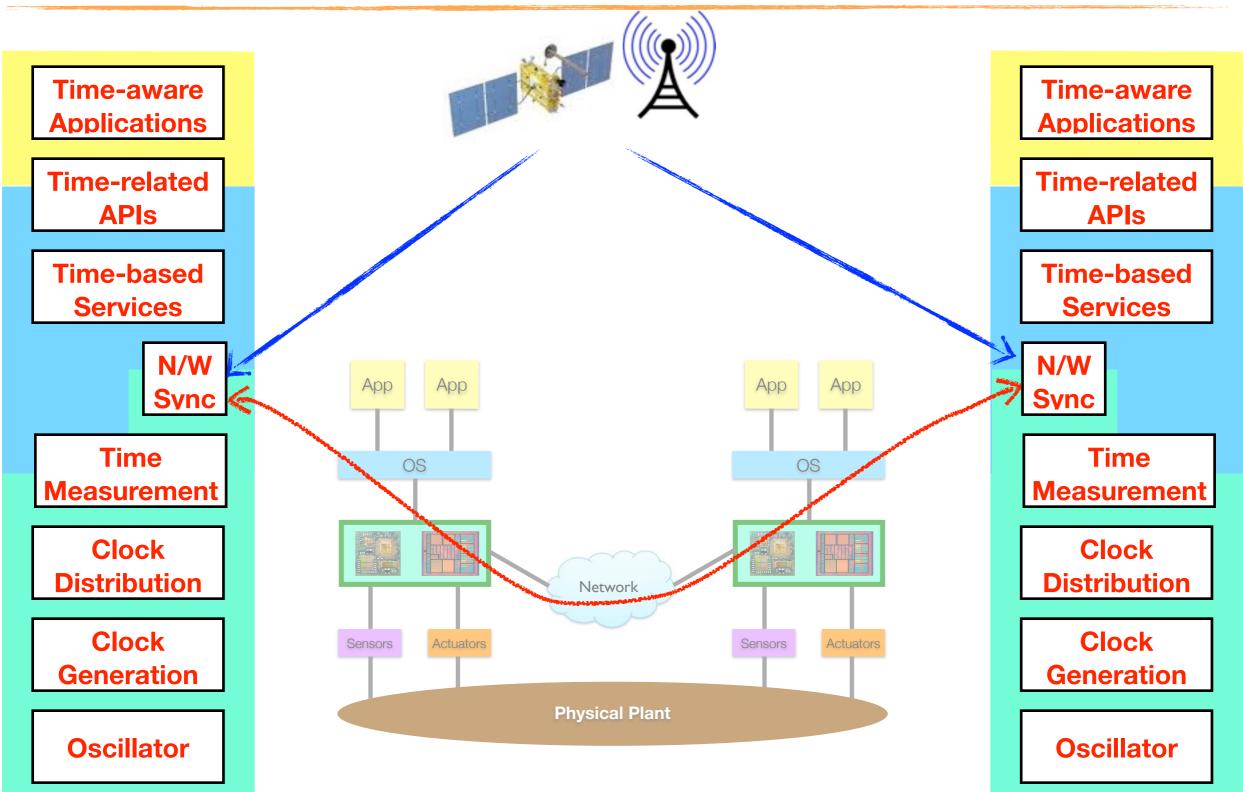


clock_gettime() What is the "time"?

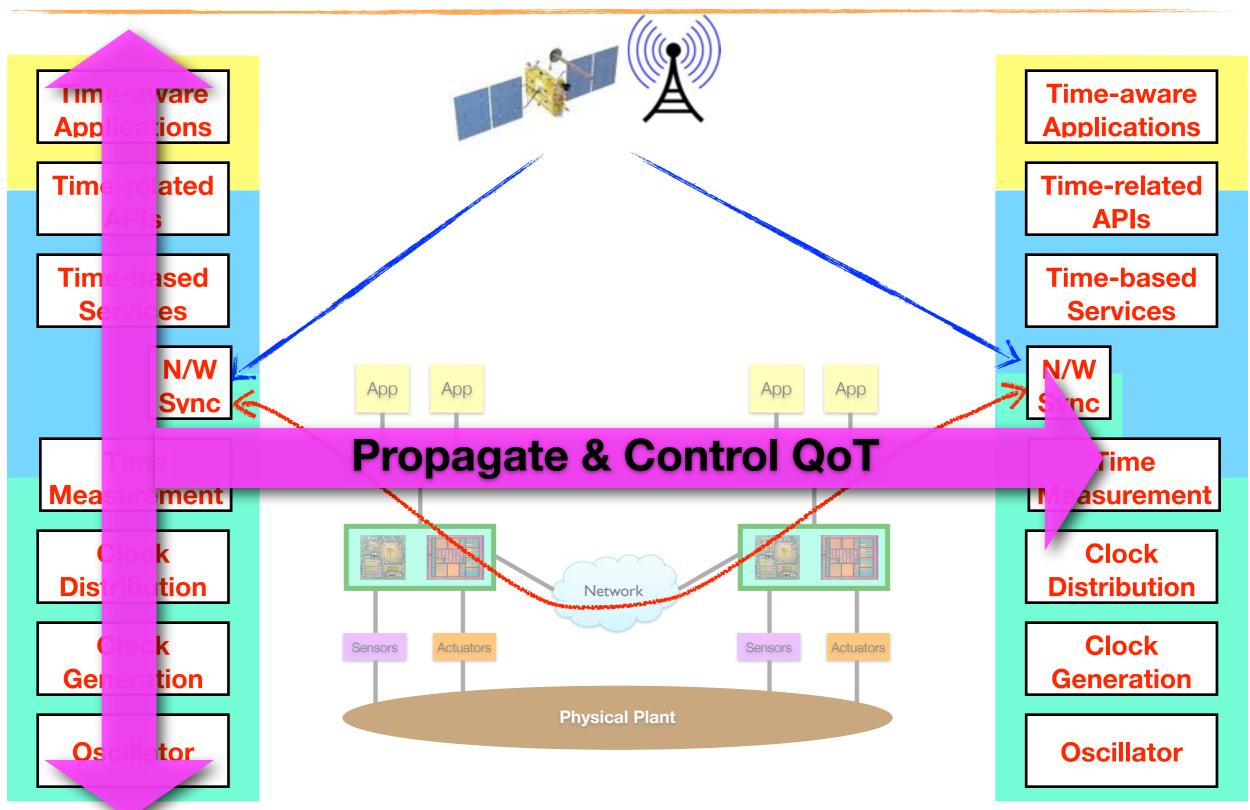
os.time() **The time is 1375599686.9 + Δ**

Our objective: transform Δ into a rich structure called "Quality of Time" (QoT) that is observed and systematically controlled throughout the system.

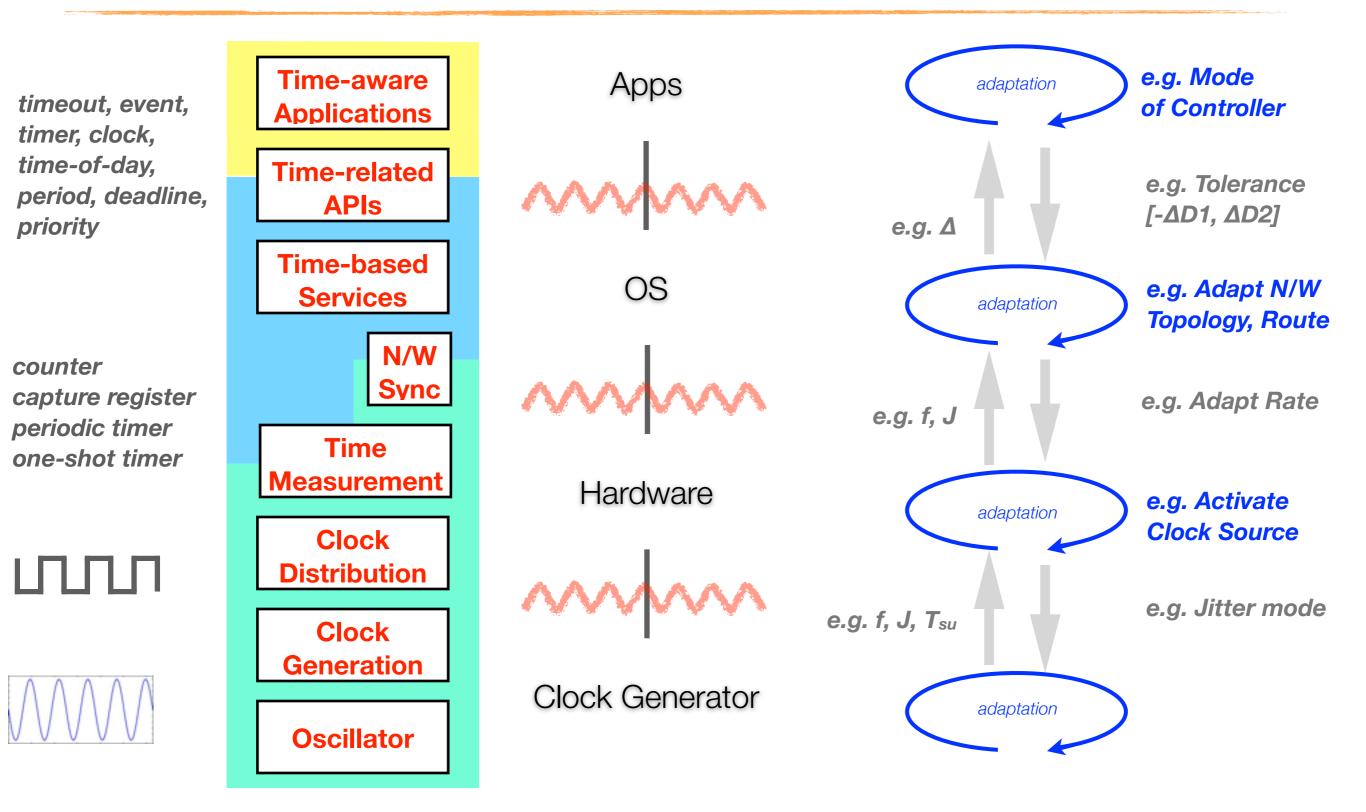
Time Information Traverses a Deep Stack



Time Information Traverses a Deep Stack



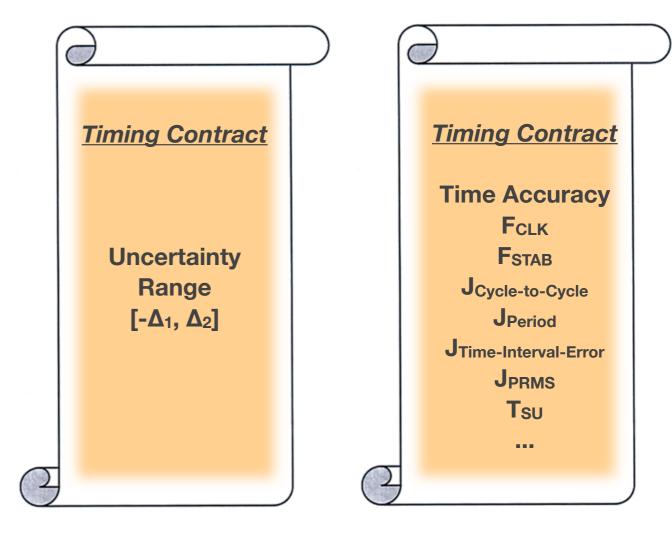
Rethinking the Time Stack From Over-design to Sense-and-Adapt



Quality of Time (QoT) Enables Contracts

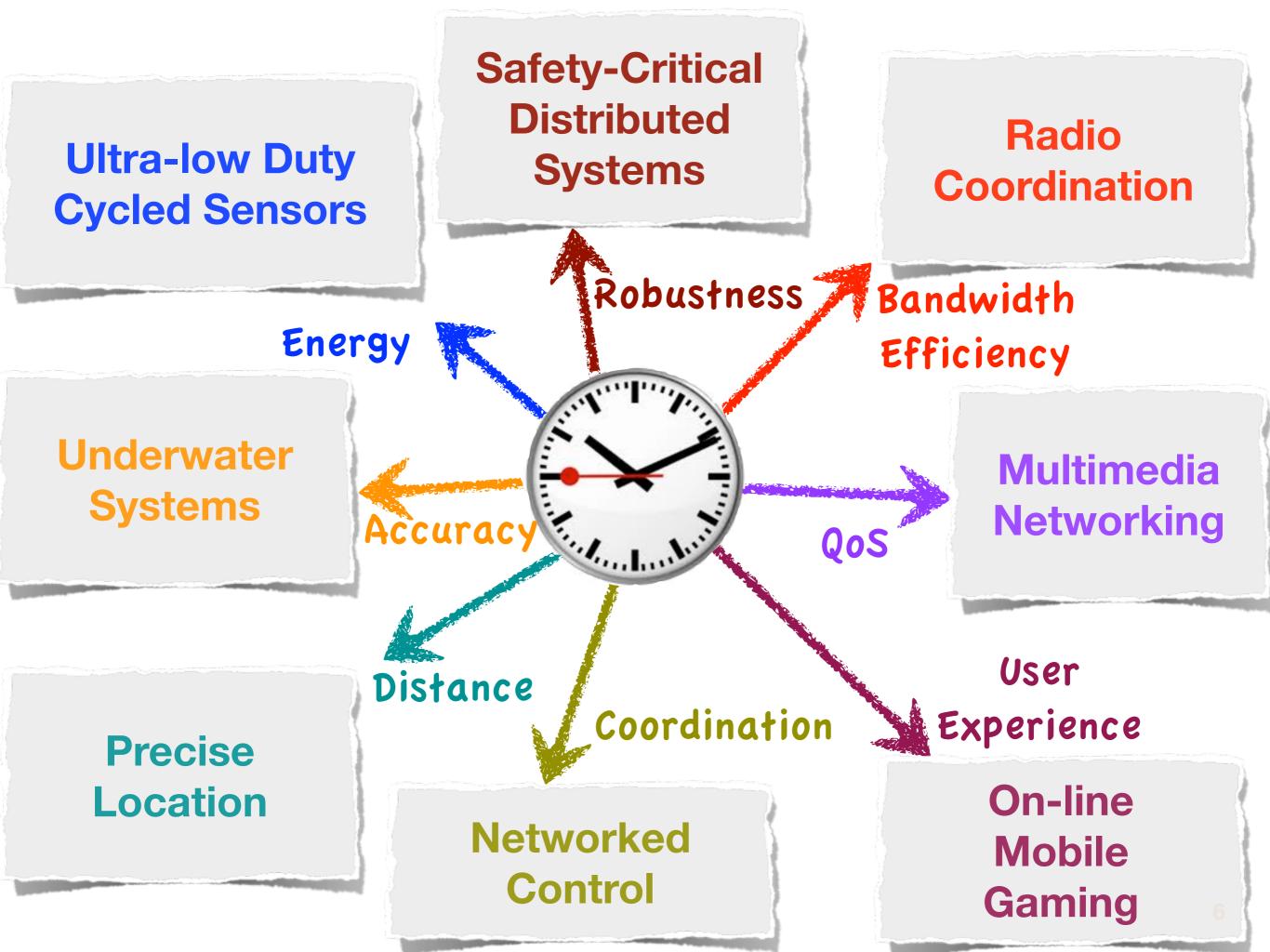
Basis of timing contracts

- Lower layer provides available QoT
 Higher layer indicates required QoT
 Exposed via APIs, HALs, and hardware interfaces
- Not a single number, but statistical parameters and ranges
- Available QoT depends on
 - Clock sources
 - Network paths
 - Network interface hardware
 - Timer/counter hardware
 - OS mechanisms
- Function of \$, J, bps, mm³ etc.



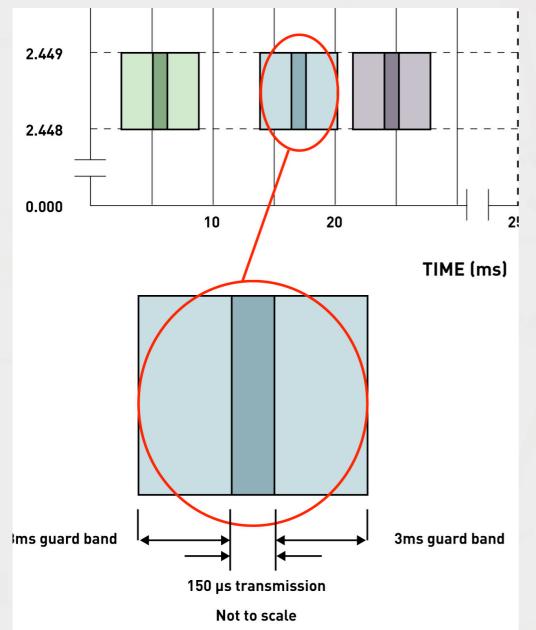
App-OS Interface

OS-HW Interface



Safety-Critical

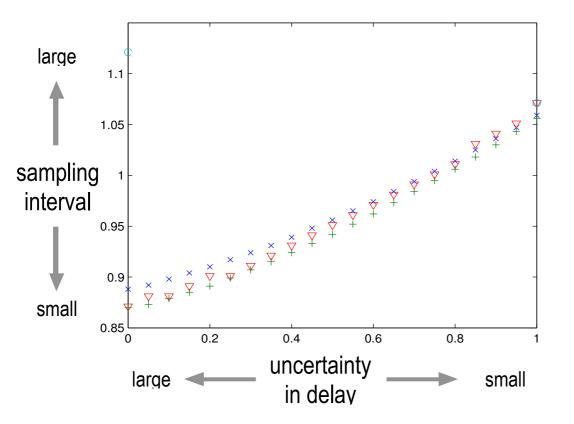
Radio Coordination in Wireless



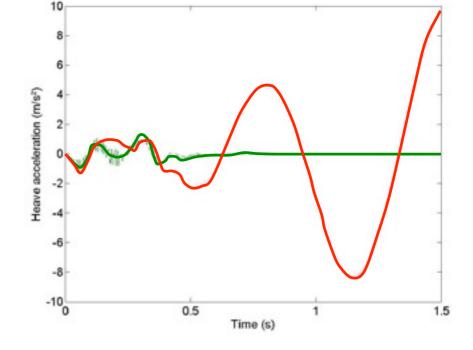
- Short-range radio protocols for D2D, wireless sensors etc.
- ► Examples: ANT, BLE, ZWAVE
- ► Low cost, power, bandwidth → High Δ → Guard bands
- Guard band proportional to relative drift & resync interval
 - ► 3 + 3 ms guard band for each 150 us message → 2.4% efficiency
 - ► Reduce guard band to 0.3 ms → 20% efficiency, or 8.2x more devices, power reduced 1.4-5x
 - Knowing QoT can enable more capacity and lower power

Safety-Critical

Networked Control



Benchmark system from [Branicky, Phillips, Zhang, ACC 2000]
 Different symbols correspond to different analysis methods



Distributed controller for car suspension system
 Two curves correspond to different CAN bus priorities

Uncertainty in delay measurement results in faster sampling
 Knowledge of QoT enables more robust and efficient controller design and operation

Untru

Safety-Critical

Precise Location in IoT



AT86RF233



- New low-power radios capable of distance measurement via phase measurement
- Jitter in clock due to PLL affects distance accuracy: low jitter PLL uses power while averaging wastes bandwidth
- Stability requirements on clock change over time
- Dynamically scaling QoT (power vs. jitter of PLL) can reduce distance error (from cms to mms) while retaining low-power rest of the time

Project Activities

<u>Thrust 2</u>

Mechanisms and Interfaces for QoT-aware Applications

Thrust 1

Autotuning Time Service for Efficient & Resilient QoT <u>Thrust 4</u> Experimental Testbeds <u>Thrust 5</u> Education & Outreach

<u>Thrust 3</u>

Circuit and Architecture Support for QoT Adaptation

Project Activities

Thrust 2

Mechanisms and Interfaces for QoT-aware Applications

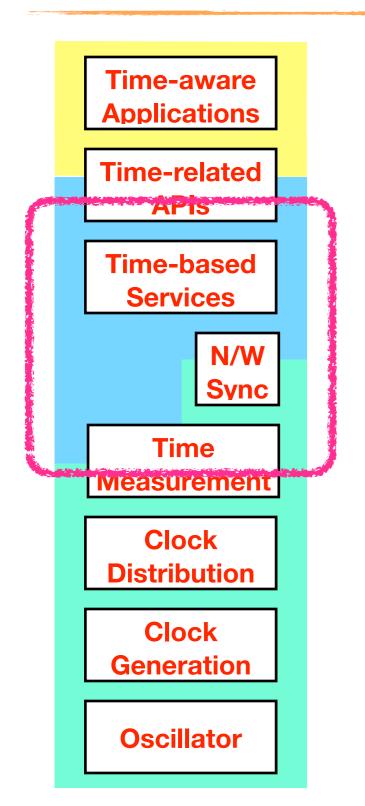
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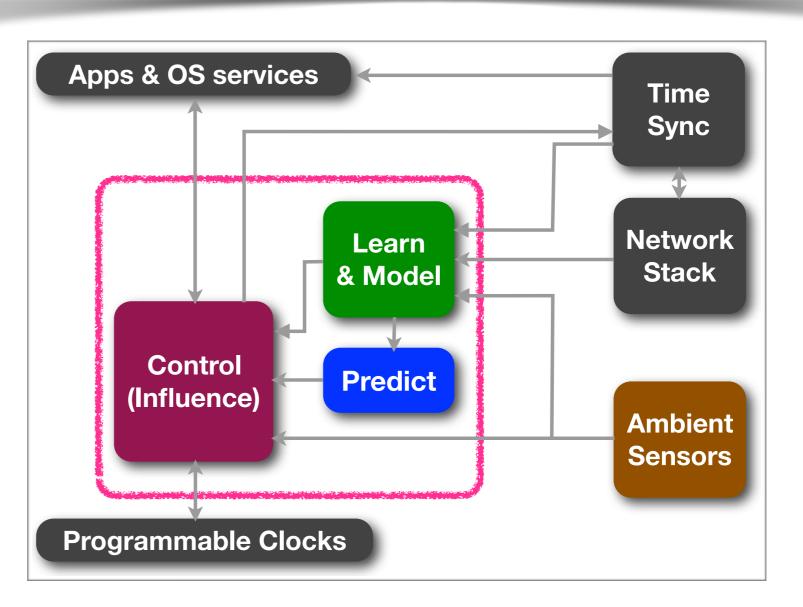
Thrust 3

Circuit and Architecture Support for QoT Adaptation

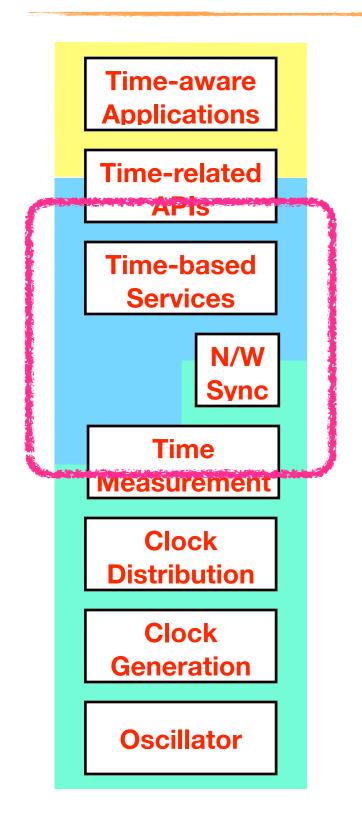
Autotuning Time Service



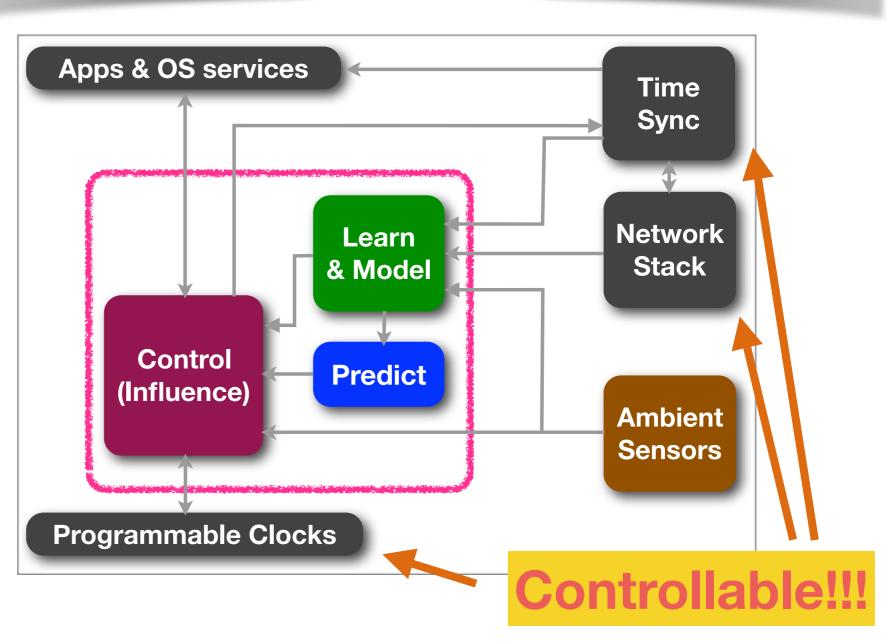
QoT = f (clock sources, network, ambient)



Autotuning Time Service

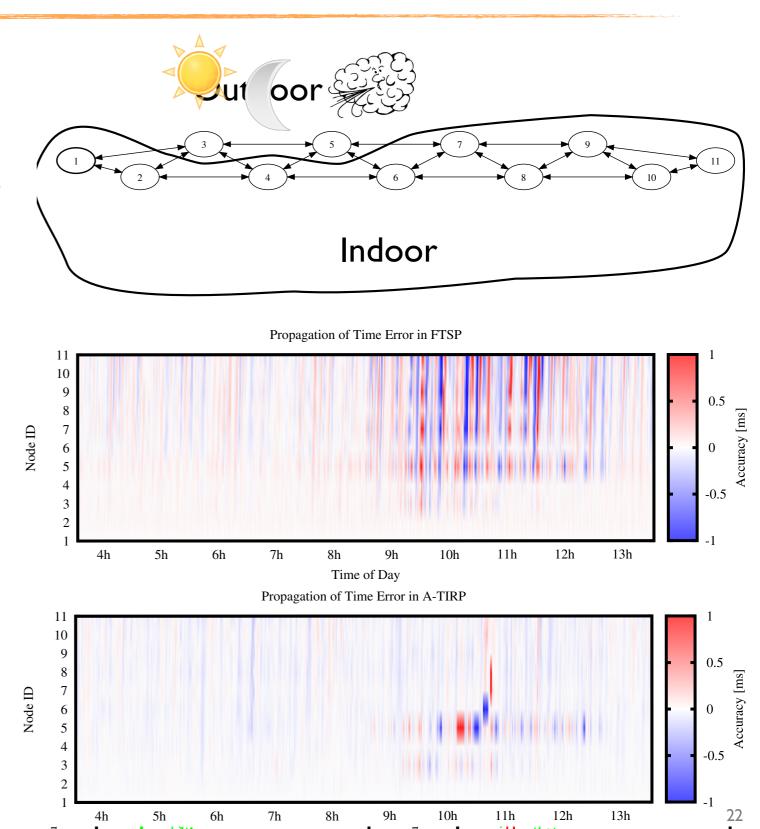


QoT = f (clock sources, network, ambient)

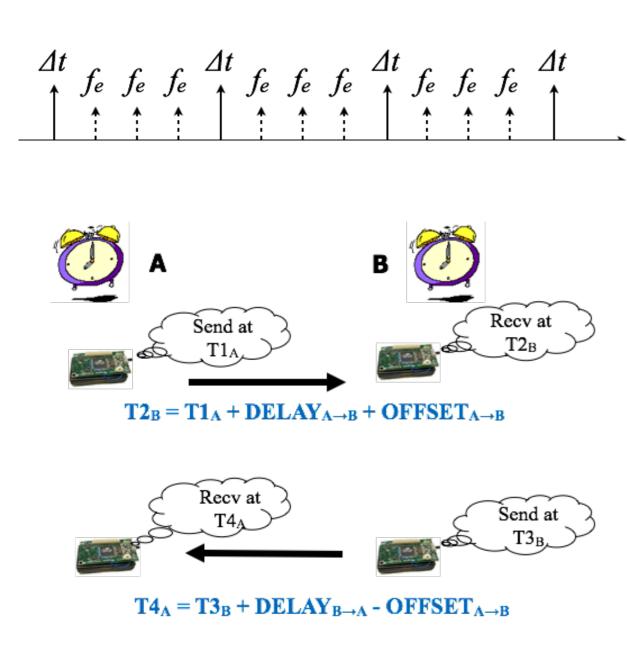


Tunable Time Sync for Multihop Wireless

- Time in multi-hop networks
 - Nodes have different QoTs
 - Paths have different characteristics
 - Intermediate nodes may misbehave
 - Path subject to "meaconing" attacks
 - Errors propagate multiplicatively
 - Standard routing uses link quality metric: suboptimal for QoT
- Time Information Routing Protocol (TIRP)
 - Selects the node with stable clocks and routes tine information around nodes with unstable clocks
- Next steps
 - General QoT metrics
 - Optimally fuse multiple references,
 - Adapt messaging based on node and path characteristics

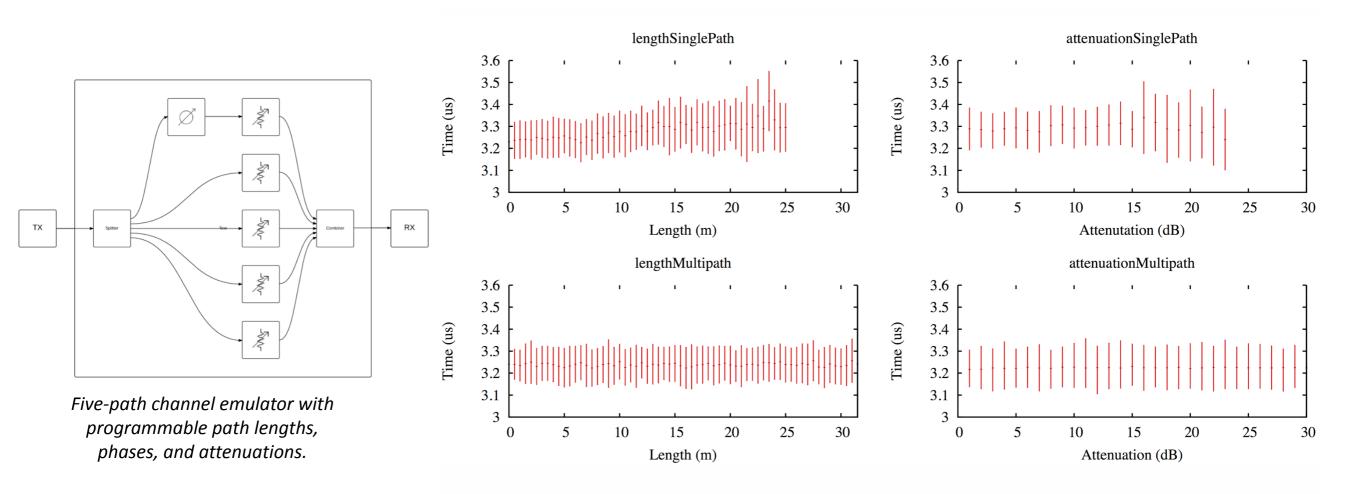


Tunable Time Sync for Multihop Wireless (contd.)





Measuring Impact of RF Channel on QoT



- TI CC2420 with SFD signal, and an RF Channel emulator for different distances, interference, and multi-path scenarios
- Even in heavy multi path environments, and at high path attenuation, SFD accuracy is stable down to a few hundred ns.

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Circuit and Architecture Support for QoT Adaptation

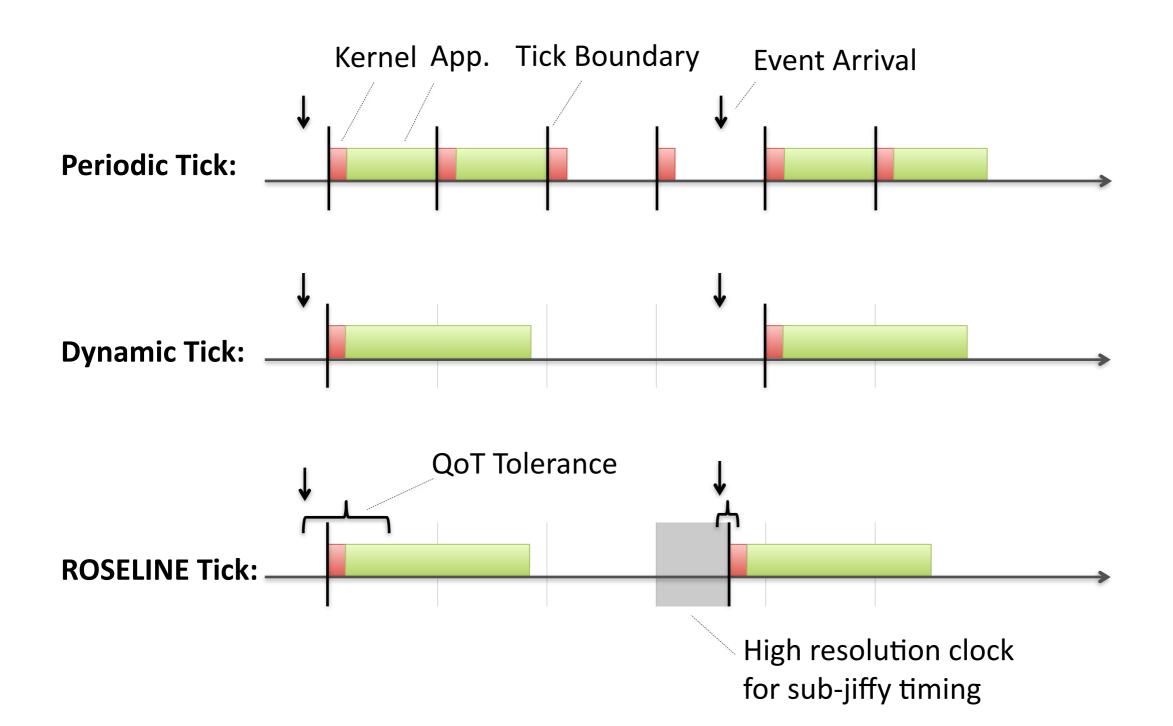
QoT at the Application-System Interface

- Applications express rich timing properties
 - Period, deadline, worst-case execution: {T, D, C}
 - Permit tolerance in specification: {T, $[-\Delta T_1, \Delta T_2]$, D, $[-\Delta D_1, \Delta D_2]$, C}
- OS and compiler use tolerance to schedule resources, control clock source and adapt time synchronization protocol settings
- Temporal fault management can be implemented as a part of exception handling in PL

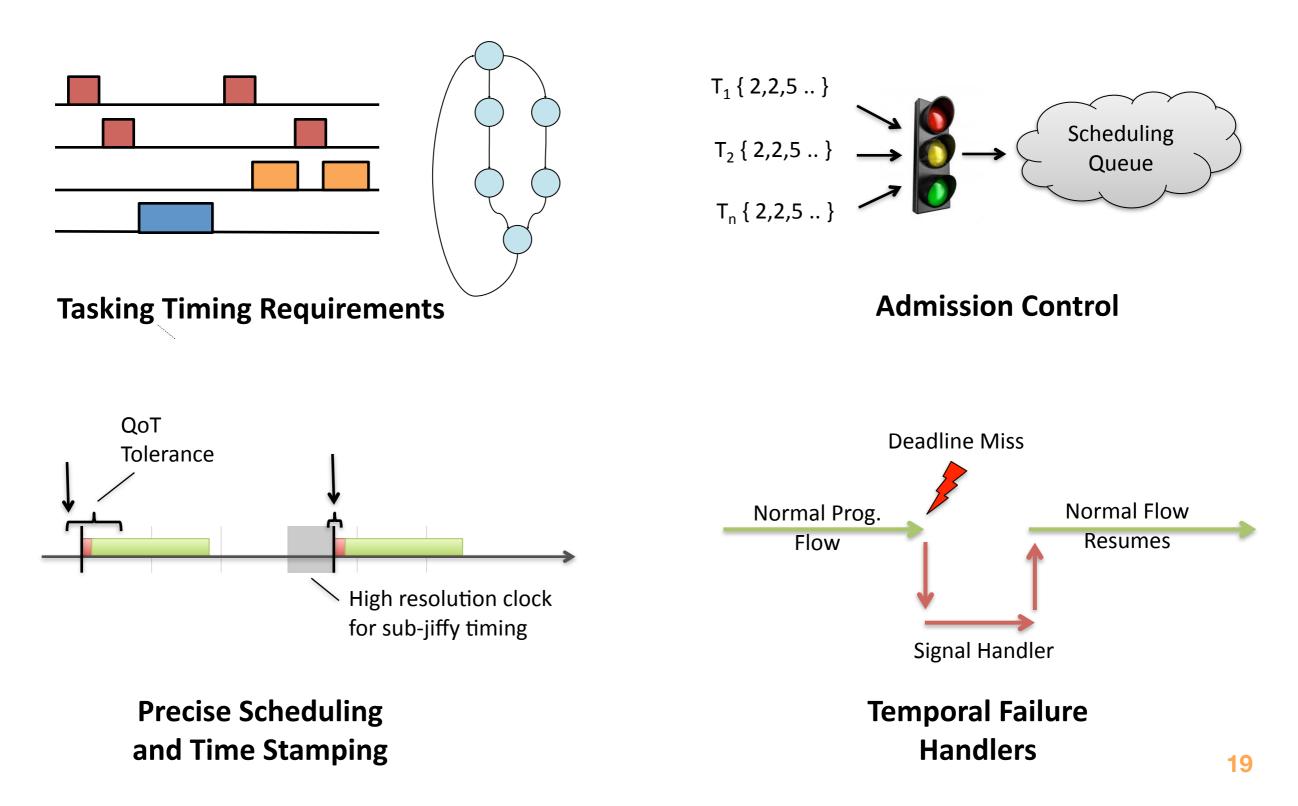
Application A								Application A				1			
Background Task B		I			Ι			Background Task B	1	Ι	I	Ι	Ι	I.	
Background Task C		1	I					Background Task C			1		Ι	1	
Application D	1			I		Ι		Application D	1		Ι	Ι		Ι	
Power Use					\mathcal{M}	\sim		Power Use							
			Time	time Pr CO	alesc	ing in	Mac C	S X Mavericks	(Ref:	Appl	e)	time			17

Gupta & Rowe

Rethinking the OS Tick

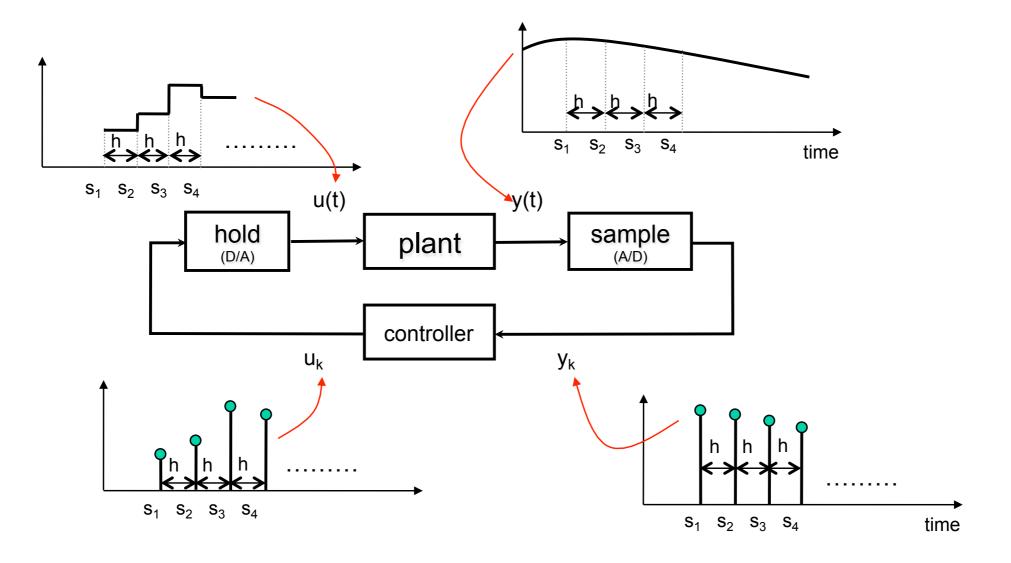


QoT-aware OS APIs and PL Abstractions



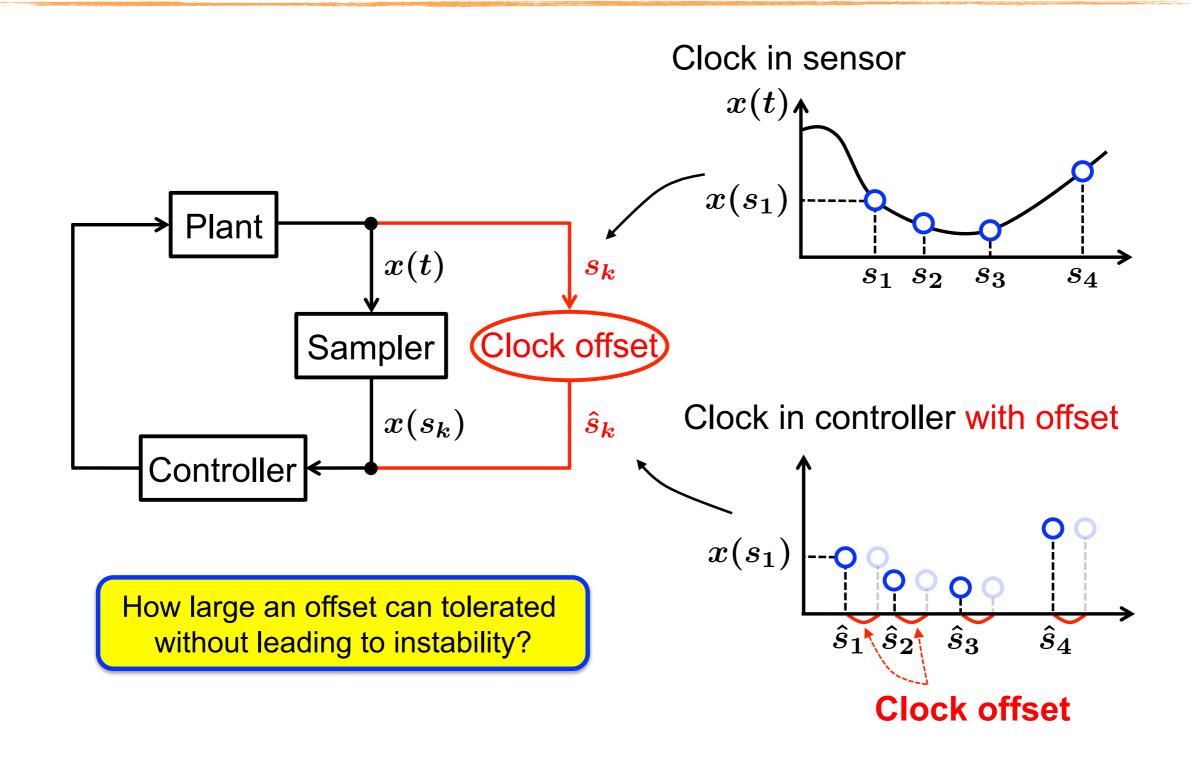
T2: Mechanisms & Interfaces for QoT Aware Applications

Digital Control Applications: Classical Synchronous Model

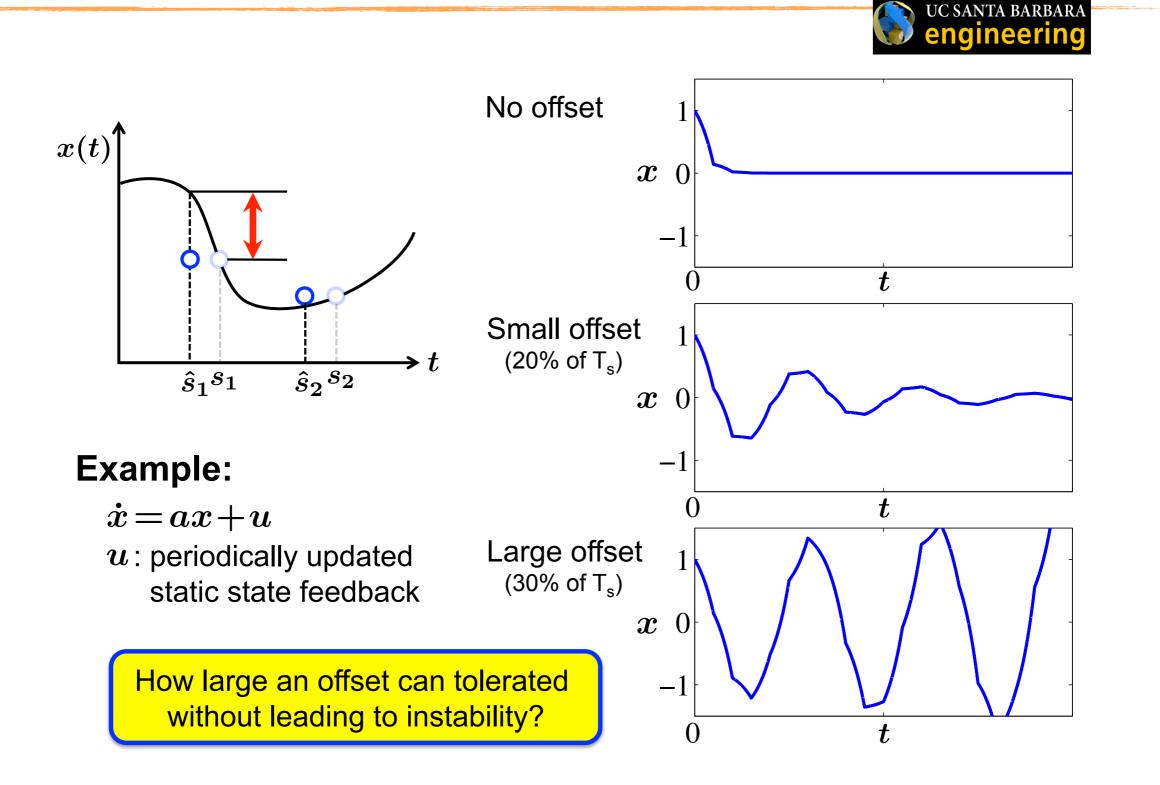


- Constant sampling time
- Sampling synchronized across nodes
- Negligible transmission delays

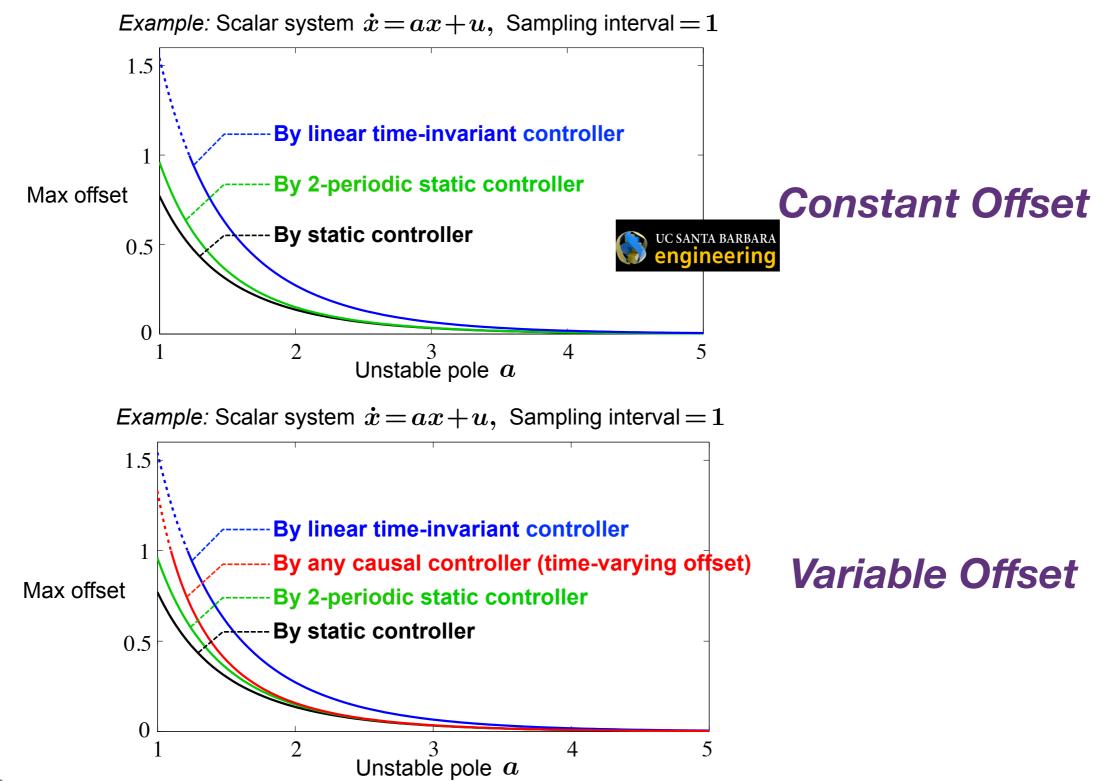
Impact of Time Synchronization Errors (due to Sensor Interface and Network)



Impact of Time Synchronization Errors



Initial Result: Maximum Allowable Clock Offset



Hespanha

Project Activities

<u>Thrust 2</u>

Mechanisms and Interfaces for QoT-aware Applications

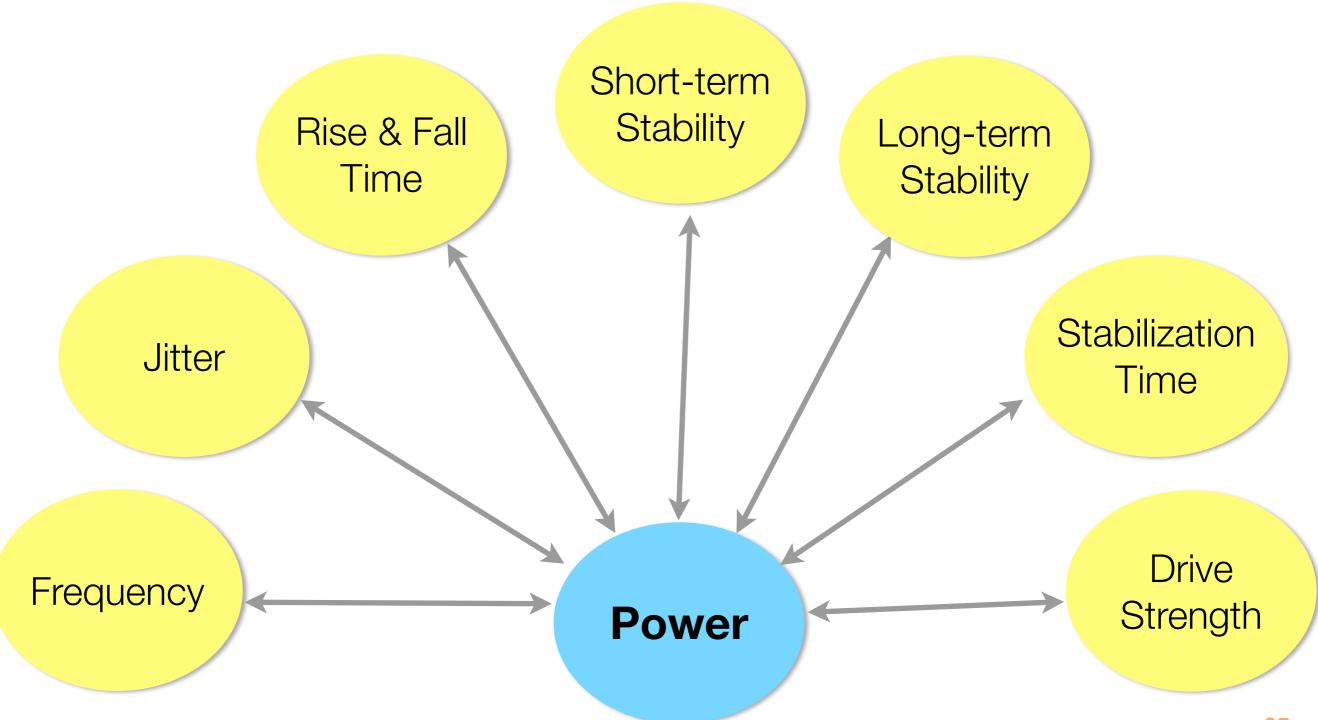
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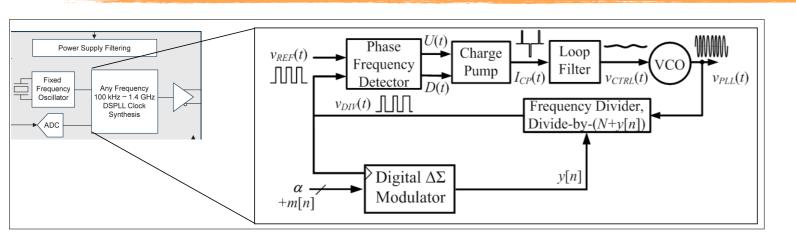
<u>Thrust 3</u>

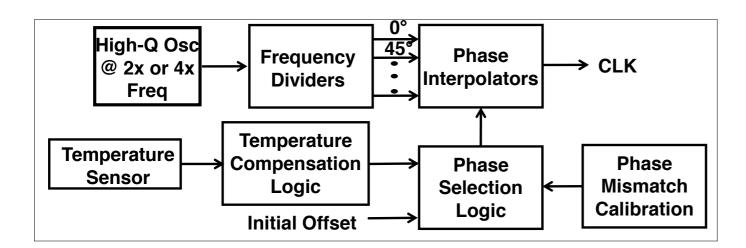
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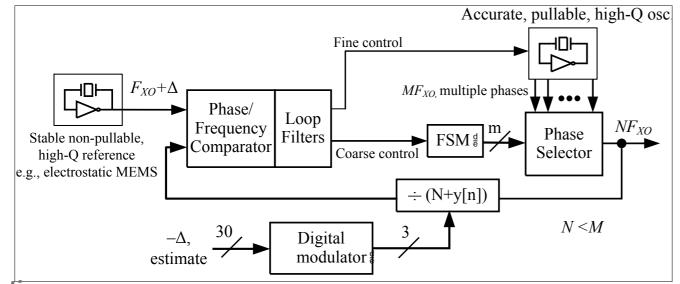
Highly Programmable Clock Generators with *Dynamically Tunable QoT*



Roseline Approach: Efficient Controllability at the Clock Sources







Highly Programmable VCTCXO

- Digital frequency programmability
- power-performance programmability in the fractional-N PLL
- Means of conveying "quality information" to higher layers

PLL-Less Synchronization

- Fractional-N PLL has programmability and compensation, but adds noise and power; High-Q oscillators have very limited pulling range
- Open loop phase switching

Multi-resonator Clocks

- Stability vs. Pullability tension
- Synchronize a stable (e.g. electrostatic MEMS) with a pullable (e.g. piezoelectric MEMS) using a fractional-N PLL

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MEMS Resonators & Si Integration

Project Activities

Thrust 2

Mechanisms and Interfaces for QoT-aware Applications

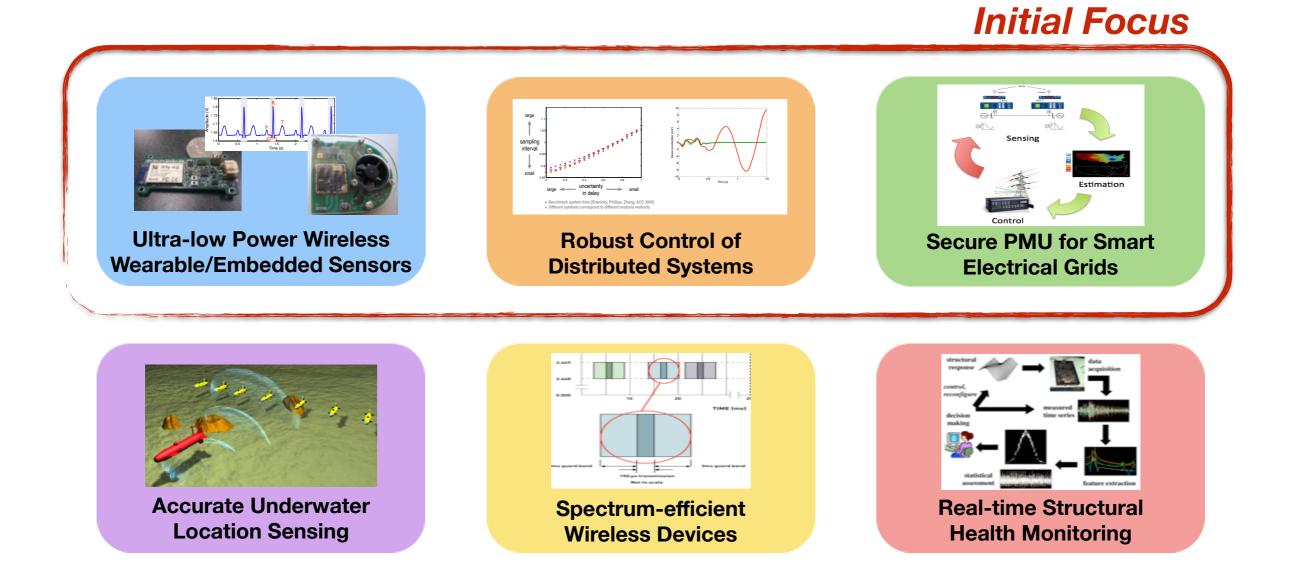
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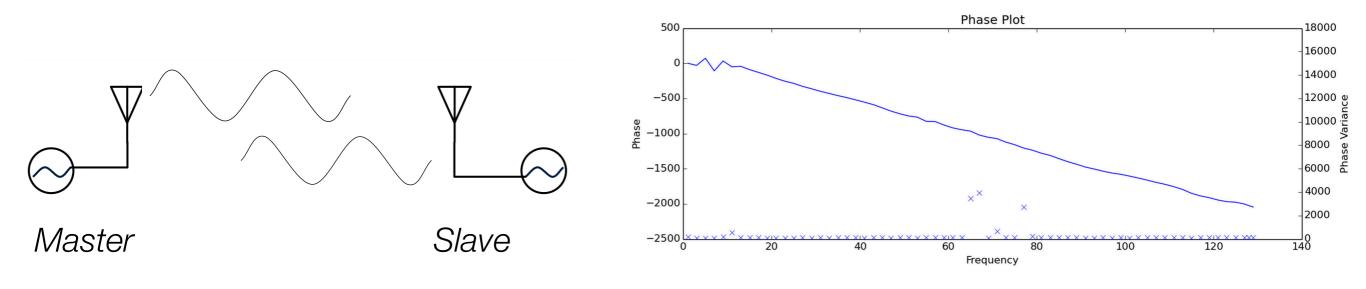
Circuit and Architecture Support for QoT Adaptation <u>Thrust 4</u> Experimental Testbeds Thrust 5 Education & Outreach

Application Testbeds



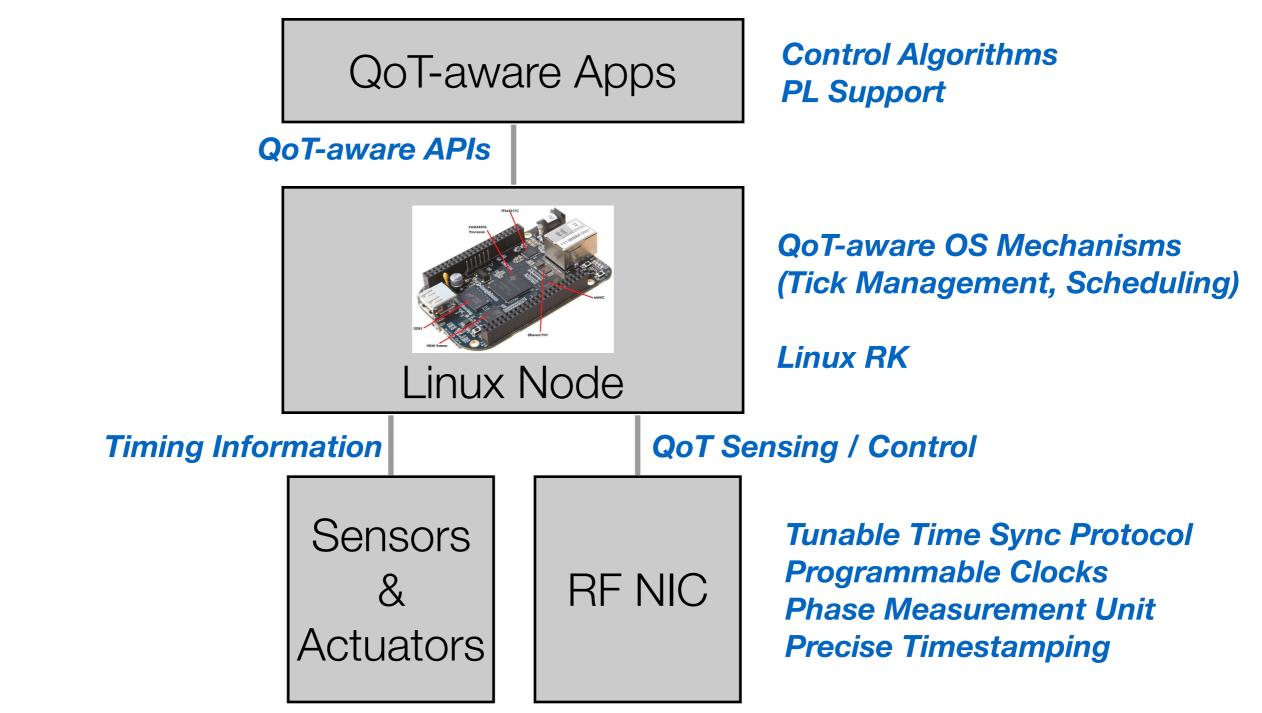
Example: Wireless Sensors with RF Precise Phase Difference Measurement

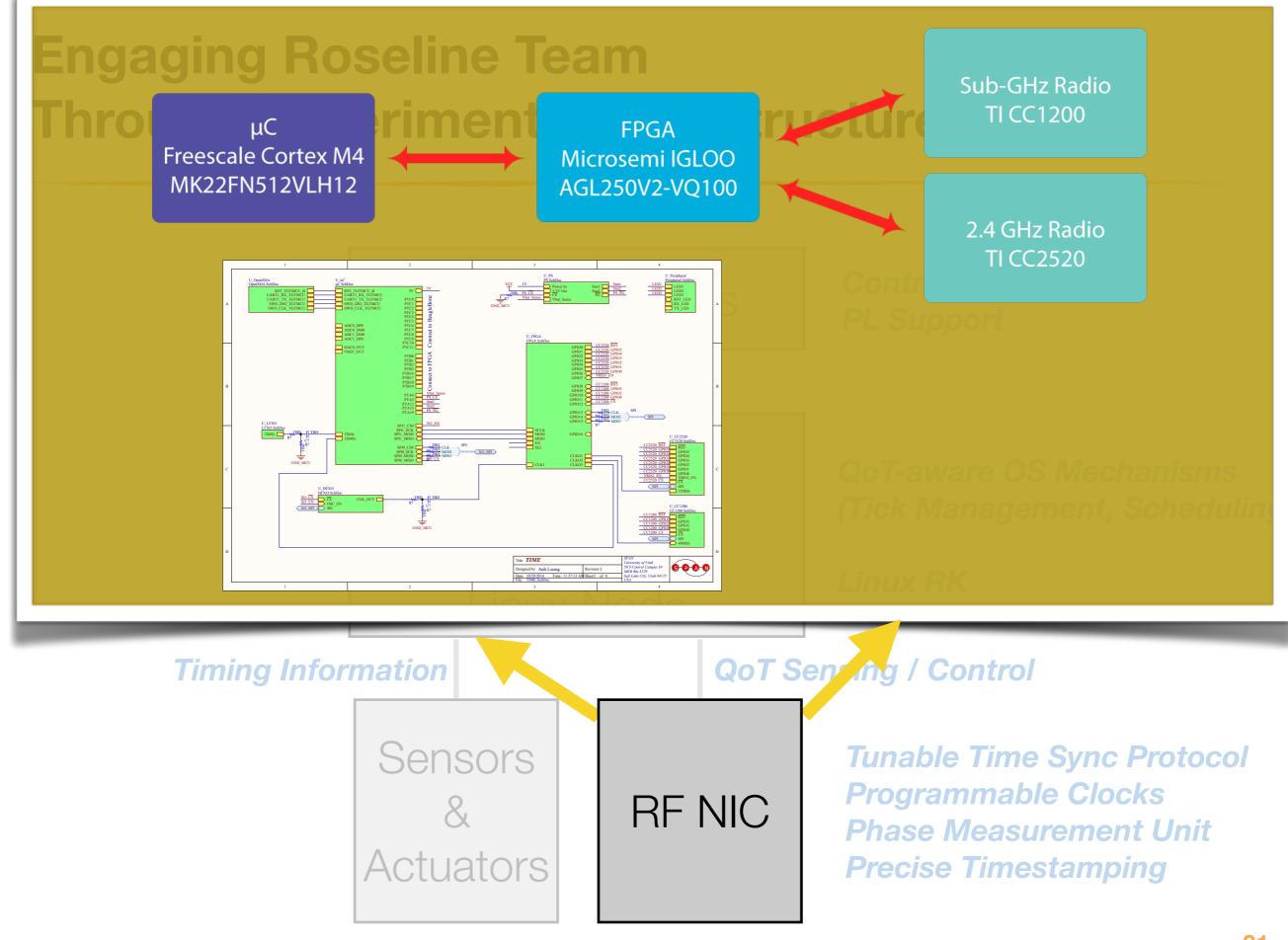
Active reflector for precise inter-node distance measurement



- Rapid and precise clock frequency synchronization
- Current activities: (i) Phase synchrony, (ii) Joint time and location, (iii) Impact of clock quality
- Promise: capacity increase in communication (distributed MIMO) and sensing capabilities (distributed beamforming, precisely synchronized sampling)

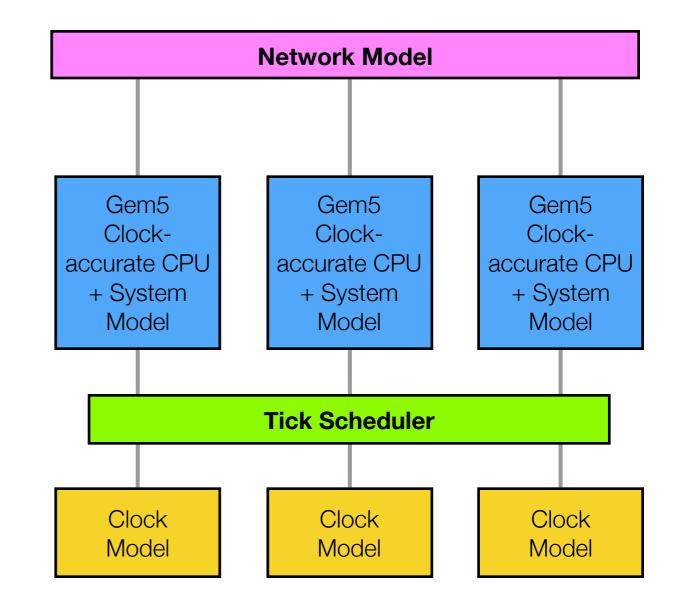
Engaging Roseline Team Through Experimental Infrastructure





Roseline Simulation Platform

- Need: study performance impact of clock and network variations, and develop software mechanisms in simulation
- Problem: simulators assume ideal clocks and global time!
- Approach: simulation environment where clock and network variations can be modeled, with Linux OS and apps
 - Based on gem5, a modular platform encompassing system-level architecture as well as processor microarchitecture



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Circuit and Architecture Support for QoT Adaptation

Bring Appreciation for the Physical into Computer Science

K-9: Inspire Passion

- Gupta/Naderi's myLab
 @ UCSD: Combine Art and Engineering with focus on Girls 7-15 (e.g. Girls Hat Day)
- Schmid's @ Utah: elementary school via CDC project on sensor-based disease tracking
- **ROSELINE will add simple actuators** & control to the learning experience







10-12: Challenge

- Los Angeles Computing Circle & HSSRP @ UCLA, COSMOS @ UCSD, Dos Pueblos Internship @ UCSB
- Strong emphasis on physicallybased computing



• ROSELINE will add modules on time-aware computing & networking



 Metrics: # going to STEM majors, tracking & mentoring mechanisms

UG & Grad: Research

Interest & Reusable Artifacts

- Collaboratively developed course modules and ROSELINE CPS toolkit
- CPS Education Initiative via CPS-VO
- Research experience for younger undergraduate students
- On-line course (Coursera)
- Metrics: # of UGs going toMS/PhD



CPS Community: Engage

STime -

Interacting

with TAACCS

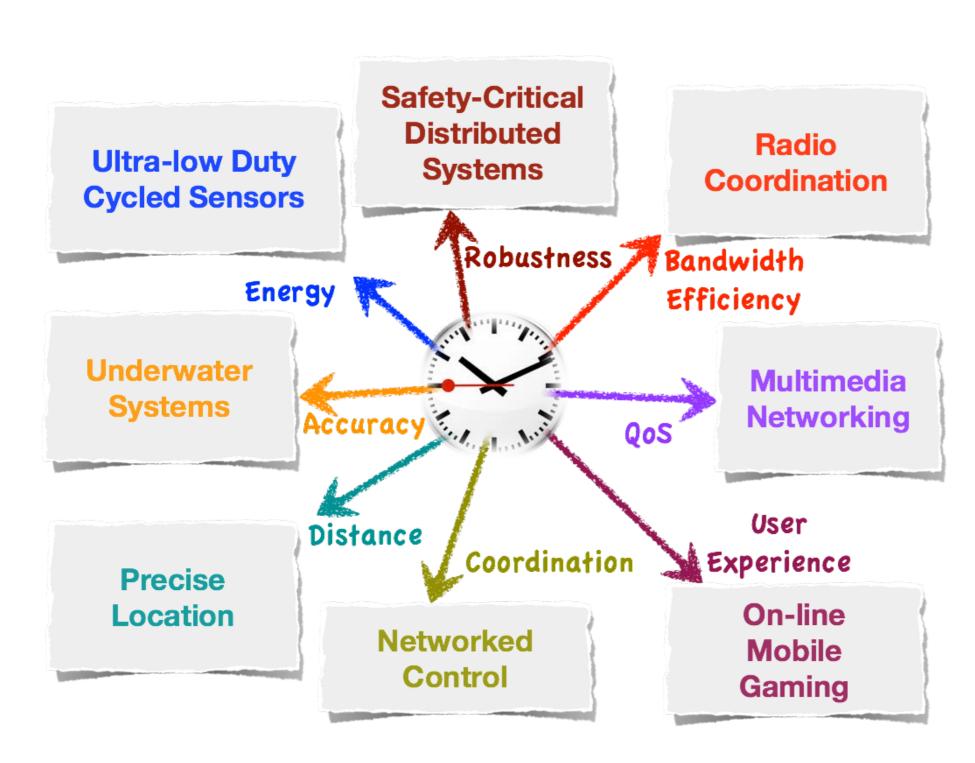
@ NIST/CMU

INSTRUMENTS

- Dissemination of tools, designs, data, testbeds, & courseware via CPS-VO
- Workshop @ CPSWeek on cross-layer time issues
- Industry engagement: Atmel, Ni, SiTime, Qualcomm
- Other collaborations: IST, IIITD, LANL
- External invitees to ROSELINE Meetings



Roseline: Defining QoT and Making It Visible & Controllable across the System



Improve robustness, bandwidth, energy, buffer, location, and user experience

Enable time-centric apps in systems & domains with intrinsic time variability

Advance state-of-theart in clocking circuits and platform architectures

Drive CPS research with a deeper understanding of time & its system trade-offs







Thank you!





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