Provably Secure, Usable, and Performant Enclaves in Multicore Processors

CSAIL

Challenge:

- Develop strong hardwaresupported isolation of software processes, with good performance and usability.
- Prove formal security properties with the Coq proof assistant.

Solution:

- New architectural primitives for enclave-to-enclave communication
- New modular proof techniques to allow separate timing-security proofs of different hardware blocks

Ideal World Only a narrow communication channel **Enclave 1 Enclave 2** proof proof Core 1 Core 2 novel IPC Careful partitioning **Security Monitor** proof **Shared Cache** proof DRAM

Scientific Impact:

- Reusable design ideas for isolation (including w.r.t. timing channels) within complex, layered digital systems
- New techniques for rigorous, modular proof of timingsensitive security properties

Broader Impact and Broader Participation:

- Release Amazon-FPGAready secure-processor designs (and proofs), ready to be evaluated and extended.
- Involve high-school students in security research via MIT Primes program.

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