Seamless Integration of Conjoined Cyber-Physical System Properties

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Effective response and adaptation to the physical world, and rigorous management of such behaviors through programmable computational means, are mandatory features of cyber-physical systems (CPS). However, achieving such capabilities across diverse application requirements surpasses the current state of the art in system platforms and tools. Current computational platforms and tools often treat physical properties individually and in isolation from other cyber and physical attributes. For example, fabrication variations can cause even commonplace physical properties like voltage and temperature response to vary, an effect amplified by increased technology scaling. Furthermore, different physical properties may be relevant to each application, which further complicates reuse of common system hardware and software across cyber-physical applications. While individual physical properties can be measured and characterized for each application, existing platforms and tools for system development do not adequately support the expression, integration, and enforcement of system properties that span cyber and physical domains. This results in inefficient use of both cyber and physical resources, and in lower system reliability and effectiveness overall.

Our research aims to incorporate an application's signals of interest with environment conditions in the physical world, so as to enable those applications to meet their CPS requirements.

In our work to date, we have constructed 6 new prototype boards, consisting of many features that make these boards well suited for pursuing research that aims to conjoin cyber and physical properties of a system. Some of the key features of these boards are; 1) a Field Programmable Gate Array chip that allows us to use a single devices to develop system architecture that allows arbitrary divisions of application functionality between software and hardware, 2) a high end Inertial Measurement Unit for integrating physical dynamics of a system, 3) a temperature monitor, 4) onboard DRAM memory to support deployment of an OS, and 5) a wireless communication module. These new boards are now being tested and will soon be available at both Washington University and Iowa State University. The first prototype of this board has been used to perform some preliminary experiments on characterizing the response-time jitter of several software/hardware codesign divisions of a time multiplexed Proportional-Integral-Derivative (PID) control algorithm. This prototype has also been used to start evaluating its ability to track thermal profiles when placed in a thermal chamber.

Our plans call for deploying test loads on these boards that will move between articulated CPS modes of interest, while experiencing changes in the operating environment. The modes of interest include real-time, in which some of the application's tasks must meet certain deadlines to remain viable; embedded, in which the application's footprint cannot exceed a predefined size; and high-performance, in which overall time for completion should be minimized. Our environment will change with respect to its ability to absorb heat from our platform. We seek to study the extent to which the application's goals can be maintained as the operating environment deteriorates or improves. The application's functionality is deployed both in hardware and software: the platform contains an FPGA that can be configured to implement System on Chip (SoC) architectures composed of both a standard 32-bit processor to execute software, and any custom digital circuits we wish to evaluate. As the environment loses its ability to absorb heat, the application must adapt so as to avoid physical destruction of the platform.

Our plans also call for investigating how standard collections objects can adapt dynamically to the modes of execution articulated above. We have thus far explored small-footprint and real-time implementations of a hash table, but our larger goal is to formulate collection objects that can move with guarantees between real-time, embedded, and high-performance operation.