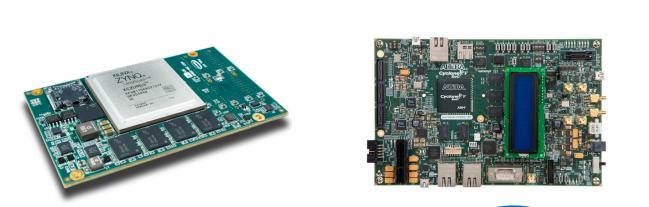
Security of Heterogeneous CPU-FPGA Systems

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Department of ECE, Rutgers University

Project URL: https://github.com/hwsel/hisa

CPU-FPGA Heterogenous System

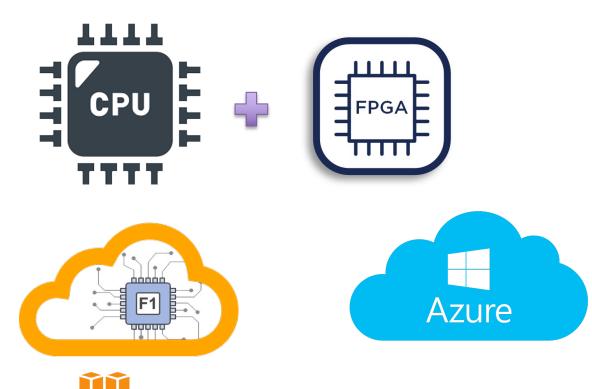




System on Chip



PC/Server



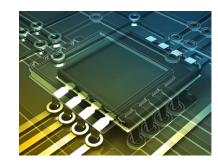
Cloud

Problem Space

Traditional Hardware Security



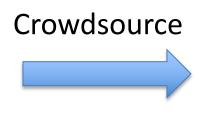


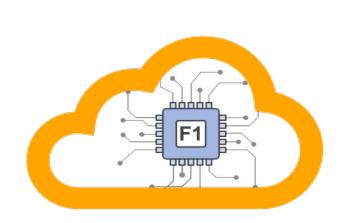


IC Manufacturing



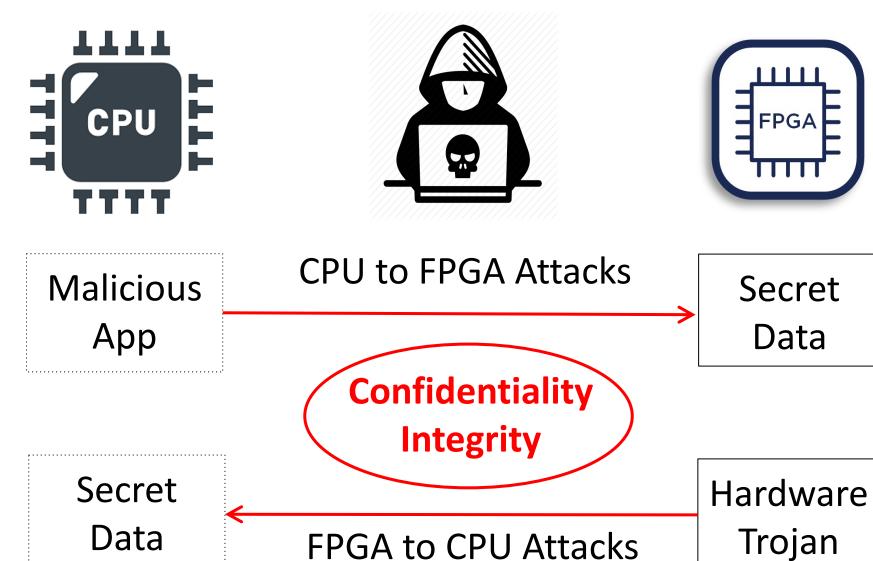




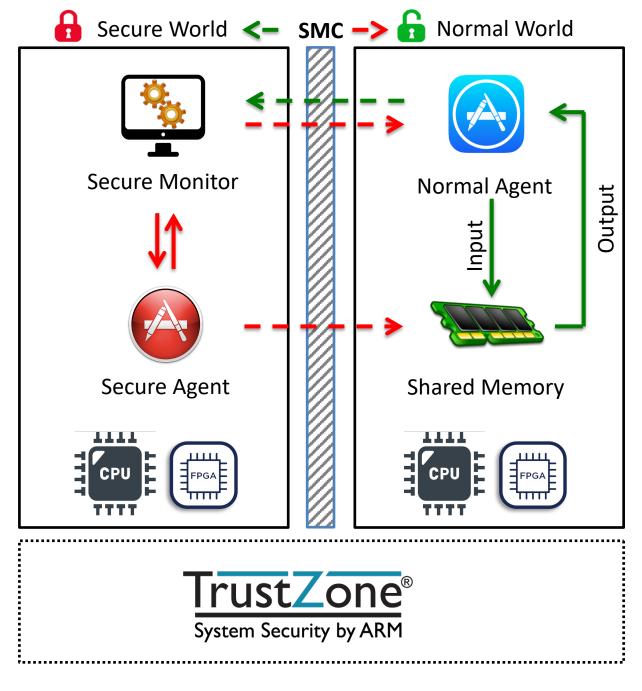


CPU-FPGA Security Challenges

Microsoft



Build the CPU-FPGA Fence

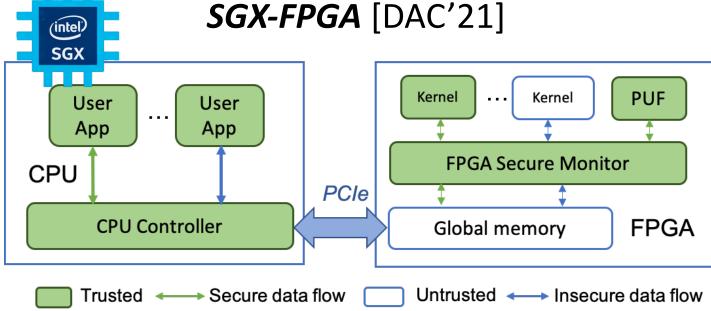


HISA [ICCAD'18]

ApproVer: Approximate Verification **CPU** Original Computation **Temporal Spatial** Approx. Approx. Verifier **FPGA** Untrusted **IP Core** [AsianHOST'19]

	Spatial Defense	Temporal Defense
Baseline	36	1
NoTrojan	31.84 (-11.56%)	1.02 (+2.00%)
STrojan	0 (-100%)	0 (-100%)

TZSlicer: Easy Programming **Tainted** Input Variables Vectors Source Program **Resource Constraints User Input TZSlicer** Program Slice **Taint** Optimizer Analyzer Slicer **HISA** Secure Normal Slice Slice [HOST'18]



Broader Impact: Society

- Cloud service providers
- Accelerator designers
- Users requiring secure high performance computing

Broader Impact: Education

- Hardware security course at **Rutgers University**
- Two female PhD students focusing on this research

Broader Impact: Applications

- Secure multimedia systems
- Secure Al/machine learning
- Secure scientific computing

