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EAGER: Cybermanufacturing: Software/ Hardware Combined Acceleration for 3D Printing in Mass Customization

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1. Computer Science & Engineering

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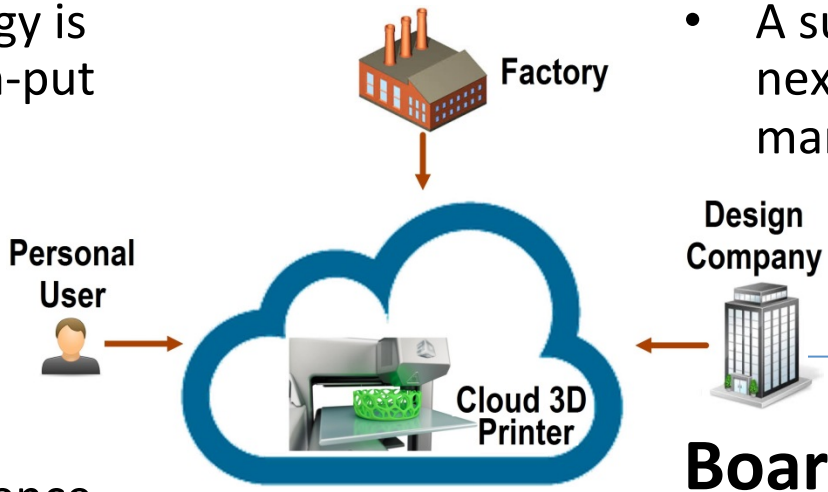
National Science Foundation
WHERE DISCOVERIES BEGIN

envisionTEC

EAGER: Cybermanufacturing: Software/Hardware Combined Acceleration for 3D Printing in Mass Customization

Challenges:

- 3D printing technology is facing a new through-put challenge.



Scientific Impacts:

- A sustainable solution for next-generation manufacturing centers;

Solutions:

- A new Computer-Science approach to accelerate 3D printing in various domains.

Boarder Impacts:

- Reduce the cost of products;
- Promote education in next-generation manufacturing;

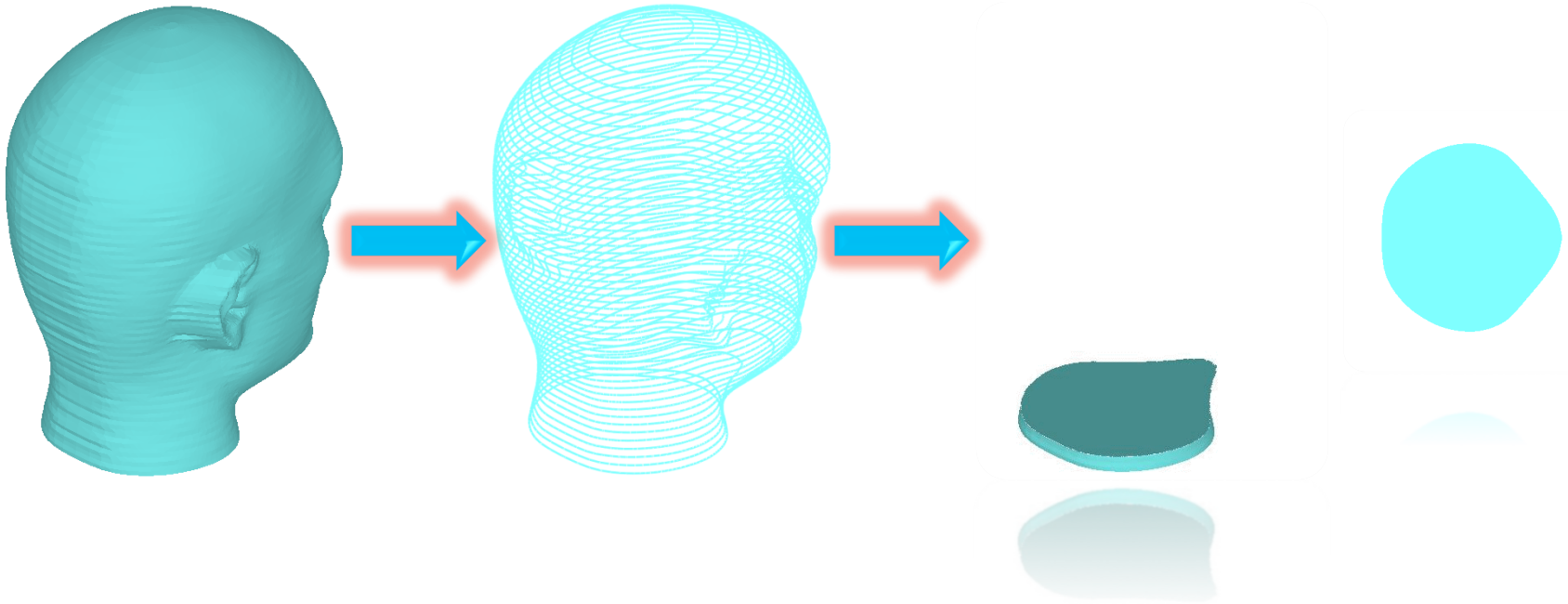
Project info (CNS-1547167, Computer Science in SUNY Buffalo, Investigators: Wenyao Xu, Chi Zhou, Jinhui Xu)

Applications of 3D printing

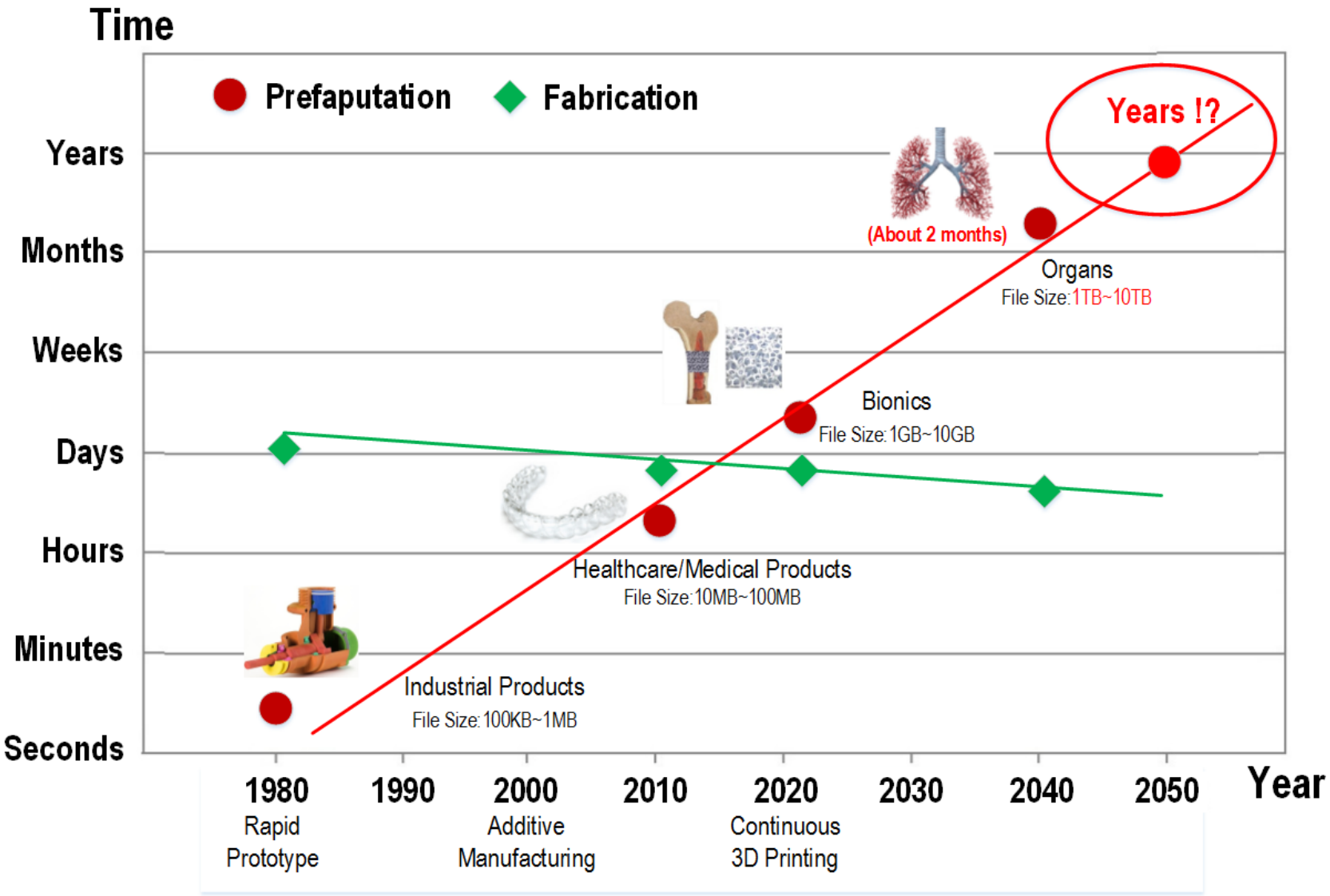
3D Printing: not just "design + fabrication"

- Prefabrication computation (short for prefaputation) is the set of computing process to prepare the input of 3D printing machine. (Similar to a compiler of a computer machine)

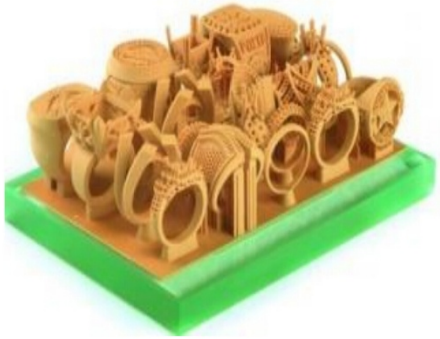
Design **Prefaputation** Fabrication



3D Printing Crisis



The common business model: Mass Customization

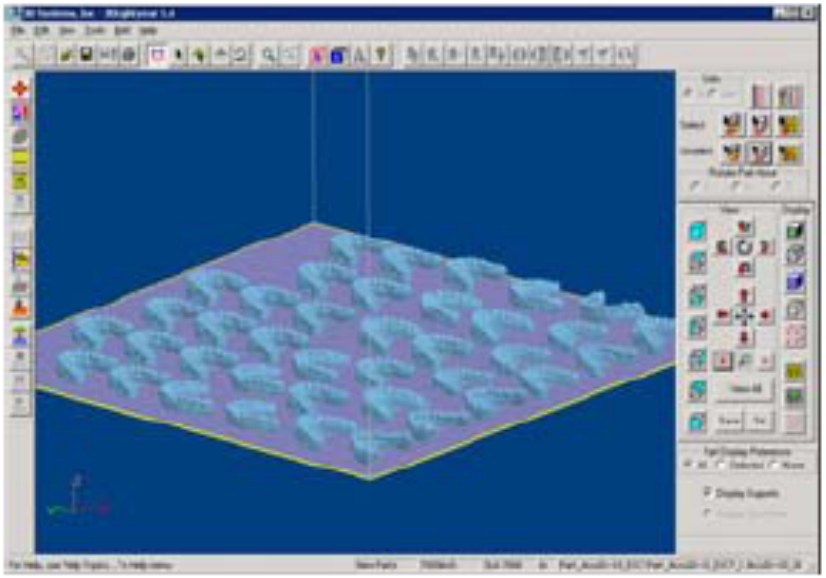


Jewelry industry

Entrainment industry

Dental industry

Medical industry



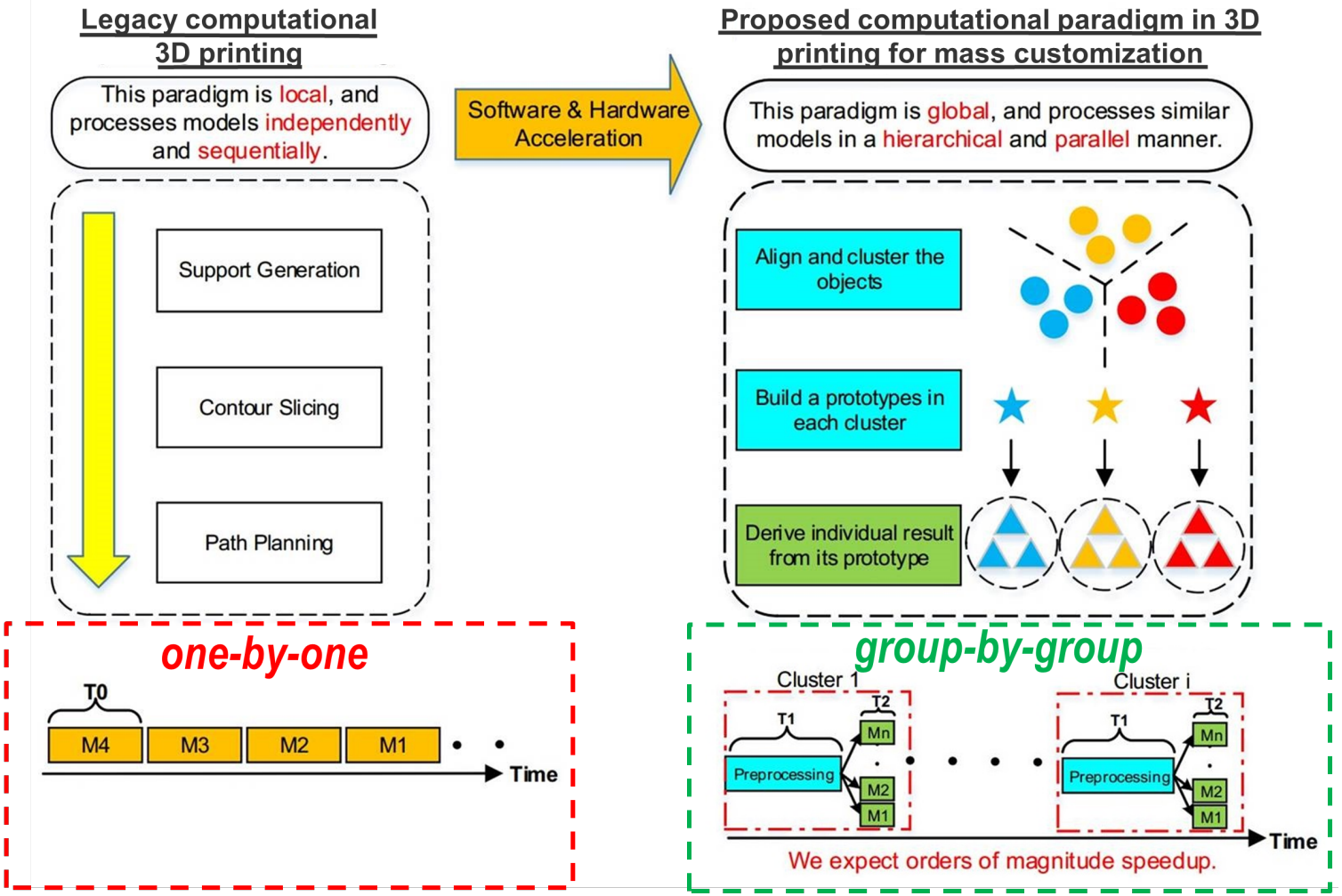
Observations and Thoughts

- ✓ In mass customization, most of the designs share the similar geometric design, so do their prefaputation results.
- ✓ ***REUSE*** the existing prefaputation results.
- ✓ The mass customization with ***REUSE*** is with a ***group-by-group*** process, instead of <u>one-by-one</u>.

Two tooth aligner models share 99% of similarity. The left is for Phase 0 – 30 days, and the right is for Phase 31 – 90 days.

A New Paradigm to Accelerate Prefaputation (1/2)

✓ **Methodology overview**

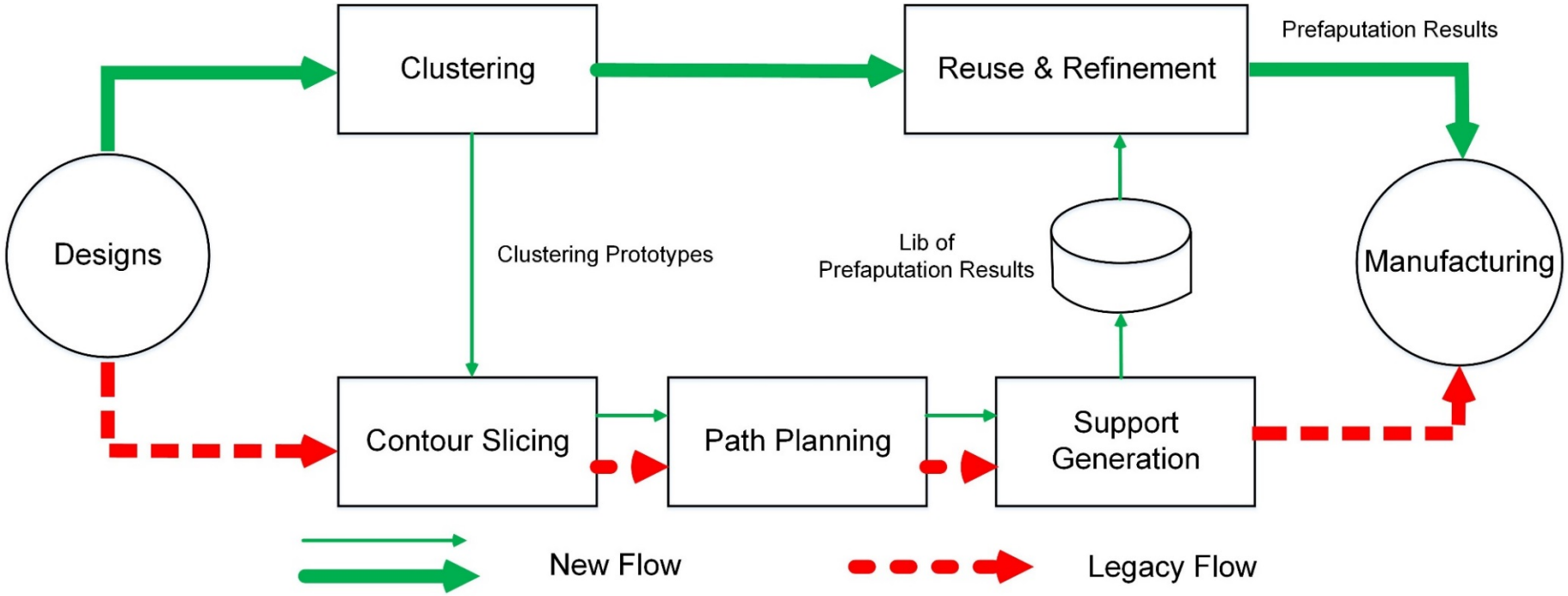


3. A New Paradigm to Accelerate Prefaputation (2/2)

✓ **Implementation overview**

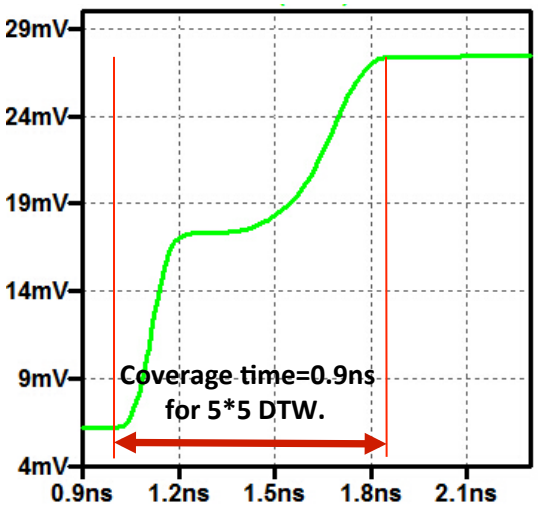
➢**Task 1: develop a suite of quality-guaranteed geometric algorithms for the new computational paradigm;**

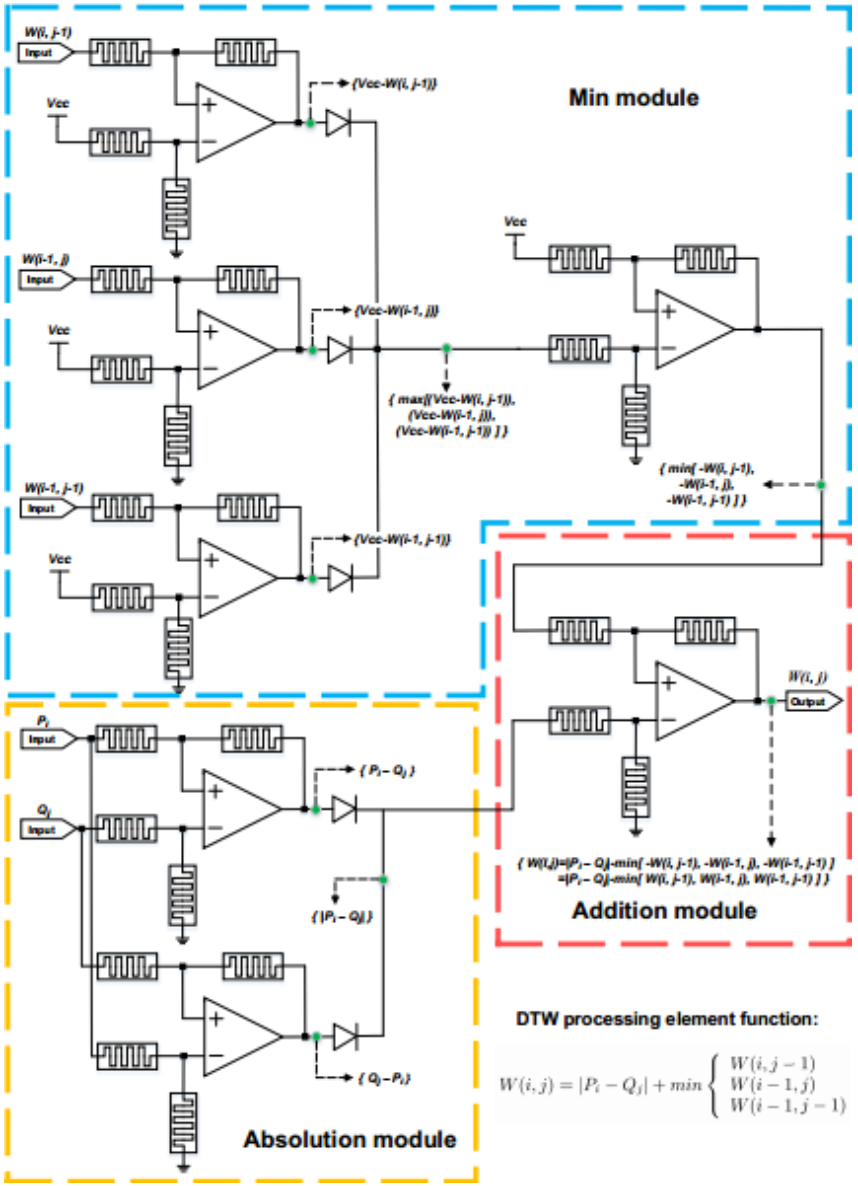
➢**Task 2: design a low-complexity accelerator-based computing platform to speedup geometrical and computing operations in the new framework.**



4. Recent Progress

- ✓ **A Memristor-Based High-throughput DTW accelerator for clustering.**
  - ➢ **The speedup is about *200x* compared with the state-of-the art DTW acceleration with FPGA[1,2].**





1. Doruk Sart, Abdullah Mueen, Walid Najjar, Eamonn Keogh, and Vit Niennattrakul. 2010. Accelerating dynamic time warping subsequence search with GPUs and FPGAs. In Data Mining (ICDM), 2010 IEEE 10th International Conference on. IEEE, 1001–1006.
2. Zilong Wang, Sitao Huang, Lanjun Wang, Hao Li, Yu Wang, and Huazhong Yang. 2013. Accelerating subsequence similarity search based on dynamic time warping distance with FPGA. In Proceedings of the ACM/SIGDA international symposium on Field programmable gate arrays. ACM, 53–62.

Thank you!

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