Time Sensitive Data Transfer using COTS Technology

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Why Commercially-off-the-shelf (COTS)?

Time Critical Systems are becoming more and more pervasive as electronics replace mechanical systems. New areas such as Big Physics, Energy Automation, Railway Systems, and Medical are paving the way for standardization in the way time critical systems are built. AFDX [3] built on COTS Ethernet is now implemented as the fly-by-wire interconnect in modern commercial aircrafts like the Airbus A380 and the Boeing 787 Dreamliner [1]. The automotive industry is currently investigating moving to Ethernet to reduce wiring and to adopt a converged network system for control and multimedia [2]. The Telecommunications sector is adopting Ethernet for cellular backhaul technology and Carrier Ethernet as a cheaper alternative to SDH/PDH and SONET [4]. This is pushing COTS Ethernet to support Time Sensitive Data Transfer (QoS) and Time Based Clock Synchronization as intrinsic features. We believe that COTS CPU architectures will follow the trend of Ethernet and enable implementation of Time Critical Systems with high determinism and predictability. The US Department of Defense and various technology companies specializing in military and aerospace applications are already focusing on exploiting COTS components whenever possible or feasible. This will lead to the replacement of proprietary technology with COTS in the majority of time critical systems in the future. Additionally new safety methods and improvements to COTS technology will enable use of such components for time critical applications in which safety and availability is of paramount importance.

Why current COTS-based systems do not meet timing requirements?

In general, COTS CPUs today are designed for asynchronous data transfer. Thus the systems are measured in terms of throughput but not in terms of timeliness. This makes the COTS CPU architectures inadequate for real time systems [11] because of the inherent variability in data transfer. If data transfer could be made predictable along with coordinated software execution, then predictability of COTS processors can be increased significantly. Making the system time triggered, with respect to data transfer, helps isochronous traffic. However, new Cyber Physical Systems need to handle both isochronous (time sensitive) as well as asynchronous (non-time sensitive) data on the same network. This increases the burden on the processors: if asynchronous data arrives at an inopportune time and contends for a shared resource (e.g., system memory), the determinism of a time critical task may be compromised. Updating the core architecture (including software and hardware) may be expensive for low cost network of COTS. We believe that COTS architecture can achieve determinism and timeliness without a thorough redesign.

What are the key technological trends to enable time sensitive behavior?

Communication Standards: Technologies like IEEE 1588 [15] have enabled precise time synchronization at the network level. IEEE 802.1Q [5] has integrated isochronous transfer through stream reservation/ forwarding as standard mechanisms in COTS Ethernet. IEEE 802.1AS [6] specifies the methodology to ensure that synchronization requirements are met for time sensitive applications across bridged local area networks. CERN is pushing strict timing and synchronization constraints into Ethernet via White Rabbit [7]. Using telecommunication standards such as Synchronous Ethernet [8] and Digital Dual Mixer Time Difference (DDTMD) [9], sub nanosecond phase synchronization can be achieved. High definition video is pushing Time Sensitive Data Transfer and time based clock synchronization into new wireless standards like IEEE 802.11ad [14]. Generation 2 of AVB is adding time based scheduling into the standard [13] to enable tighter latency and higher loop rates.

Computation Platforms: FPGA vendors like Xilinx are pushing System on Chip (SoC) architectures as COTS. Zynq [10] is an example of one such architecture. This enables building high performance Time Critical Systems using COTS technology without compromising performance. Such systems are typically integrated with COTS Ethernet technology thereby enabling Cyber Physical Systems architectures with tight synchronization.

Programming Models: The requirement of transitioning from a domain expert to a programmer is slowly disappearing as intuitive high level programming languages like LabVIEW empower domain experts in development of Time Critical Systems using COTS components (or technology).

What needs to be done in future?

We see four clear gaps that, if remedied, would enable COTS based architectures to be used successfully in all Time Critical Systems that require high predictability:

1. **(Global) Time Aware Processor Interconnects:** Technologies (e.g., IEEE 1588) have enabled precise time synchronization at the network level. However, when this time needs to be propagated into a CPU subsystem, precision is lost, since the interval between the time when a timestamp was taken by a network interface card (NIC) and the time when it is received by another device in the CPU subsystem cannot be accounted for. This needs to be addressed by building time synchronization into CPU subsystem interconnects. If all devices have a common notion of subsystem time, then any incoming global time can be correlated/ mapped to the local subsystem time without losing precision.

2. **(Sub-system) Time Aware CPUs:** In general, CPUs are not considered endpoints of system interconnect, and are integrated with the system interconnect by a vendor specific method which makes standardization of subsystem timing in the CPUs very hard. If all COTS CPUs could enable presentation of subsystem time (described in 1) into internal CPU registers, then the logic executing on the CPU could be synchronized to this subsystem time. This would enable coordination between software logic execution and data transfer with high precision thereby eliminating contention of shared elements which increases predictability.

3. **(Global) Time Aware IO Peripherals:** Control systems read data from the physical environment, process the information, and compute new data to be written to actuators. In Time Critical Systems, the reading/writing of data should be done in a timely manner at IO peripherals which must have the notion of global time for the system. This would entail reading and writing of data at precise times, to enhance predictability of IO behavior.

4. **(Data Transfer) Time Aware Memory Interfaces:** In Time Critical Systems, transfer of Time Sensitive Data across memory must be predictable. If the transfer could be offloaded by hardware, then the guarantee of higher predictability goes up considerably. It also reduces the burden of software scheduling. If all interfaces into the CPU subsystem can implement a hardware assist mechanism which can be programmed by schedulers using a common concept of time, then Time Sensitive Data transfer would become an implicit part of the system (not something that needs to be approximated). This hardware assist mechanism should be aware of asynchronous data and control related transfer in a coordinated manner so as not to compromise system predictability.

Once the above issues are addressed, time based scheduling algorithms can implement serialized access of shared resources like memory and system interconnect bus. This would make isochronous data transfer predictable (by allowing for repeatable memory accesses by all components in a system) and asynchronous data transfer efficient (by managing bandwidth sharing using a common concept of time) which would lead to better data throughput and improved (onboard) memory usage. The focus of the proposed solution is a system infrastructure that shares a notion of global time across all components and sub-components, and allows access to common resources based on the global time. We assume that the timing requirements (for applications) are captured using logical notion of time (i.e., in a platform independent manner) [12], and system-level tools automatically connect the logical time with the physical time during mapping, verification and synthesis.

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